SP Energy Networks

D-Suite

Design Guidance of D-Suite Devices

3/26/24

Future Networks

ABOUT REPORT

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Index

Glossary of Terms

TERM	DEFINITION
AC	Alternating Current.
DC	Direct Current.
DER	Distributed Energy Resource.
DNOs	Distribution Network Operators.
D-HF	Distributed Harmonic Filter.
D-SOP	Distributed Soft-open Point.
D-STATCOM	Distributed Static c Synchronous Compensator.
D-ST	Distributed Smart Transformer.
EV	Electric Vehicle.
EU	European Union.
GB	Great Britain.
GW	Giga-Watts.
HVDC	High Voltage Direct Current.
IGBT	Insulated Gate Bi-Polar Transistor.
kV	Kilo-Volts
LI	Lightning Impulse
LV	Low Voltage
MOSFET	Metal-oxide-semiconductor Field-effect Transistor
MV	Medium Voltage
MVDC	Medium Voltage DC
MVA	Mega-Volt Amps
MVAr	Reactive Mega-Volt Amps
MW	Mega-Watts
SI	Switching Impulse
SiC	Silicon Carbide
UK	United Kingdom
VSC	Voltage Source Convertor
Wh	Watt-hour
WP	Work Package

1. Executive Summary

The main purpose of this report is to provide guidance to optimaly design D-Suite devices in the Alpha stage. Control strategies, hardware optimisation design methods and protection were developed for D-suite devices, among which the most complex equipment - distributed smart transformer (D-ST), was used as an example for discussion.

The line-frequency transformer is integrated with a partially rated PED, offering enhanced flexibility for power flow control in both balanced and unbalanced scenarios. Furthermore, the PED has undergone an optimised design process, resulting in a high-power density and cost-effectiveness. To safeguard the PED against potential damage during fault conditions, comprehensive protection mechanisms have been developed. These protections are designed to ensure that the transformer's functionality remains intact even in the presence of faults, including overcurrent and overvoltage conditions.

Key outcomes of this report include:

- Effective Control Solution: The D-STs offer active power and voltage regulation capabilities within low-voltage distribution networks. This achievement is made through the incorporation of a partially rated PED into the transformer. To address unbalanced load conditions, the PED has been specifically designed to operate within a three-phase four-wire configuration. A complete simulation model has been developed to verify the effectiveness of the method.
- Optimal Hardware Design: The hardware optimisation design of power electronics converters revolves around a strategic approach to balancing power density, cost-effectiveness, and efficiency. The switching frequency has been chosen as the design parameter. Lower switching frequencies can improve efficiency by reducing switching losses but may require larger and more expensive passive components, impacting cost and power density negatively. Hence, the choice of switching frequency must strike a careful balance.
- Enhanced Protection Strategy: Protective measures have been investigated to safeguard the PED during the occurrence of the most severe external grid faults. Bypass thyristors have been incorporated into the design to shield the PED against short-circuit faults. A pre-charging circuit has been integrated to control the converter's inrush current. Varistors and a dc-link clamping circuit have been implemented to provide protection against lightning surges and switching surges.

2. Project Background

Due to the increasing uptake of Low Carbon Technologies (LCTs), the problems LV networks will experience, will mainly be voltage rise and high circuit and transformer stress, which will be compounded by large phase imbalance due to single-phase connections.

D-Suite is applying against the Improving Energy System Resilience and Robustness challenge. The project goal is to develop the D-Suite technology technical scope, seek feedback from the supplier base identified in the discovery stage, and select appropriate trial sites to test the technology.

The Alpha stage D-Suite Project plan is divided into:

- Improve the TRL, so the D-Suite technologies are more readily available.
- Encourage the D-Suite supplier market's participation in a tender Pre-Qualification Questionnaire, so DNOs can understand the indicative costs before full tender in the Beta stage.
- Select several D-Suite technology trial sites within at least one UK DNO LV network.
- Develop and verify a fully evidenced Cost Benefit Analysis through desktop study D-Suite simulation results for technical benefits and use PQQ returns for the provision of indicative costs.
- Develop training pack inputs for LV design engineers, so they can easily design LV networks with D-Suite Technologies at the network planning and investment approval stage.

The product and service provided by the project includes:

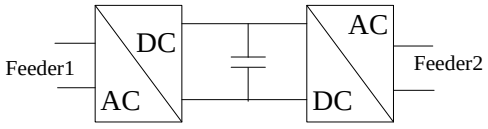
- Kickstarting the LV PED market to produce innovative low-cost D-Suite designs based on modular DC- components.
- Developing D-Suite control and protection strategies to maximize benefits and equipment safety.
- Developing D-Suite design and planning tools.
- Developing operation and safety documents for novel D-Suite technologies.

The project involves end users (network design, planning and control engineers), PED suppliers, PE consultancies, network design and standards teams, local authorities, and academic partners to ensure that the D-Suite technologies are fit for purpose at the deployment stage. A deployment of D-Suite devices at the LV voltage level, would be a first for UK DNOs and would represent a leap forward in active LV network control using PEDs.

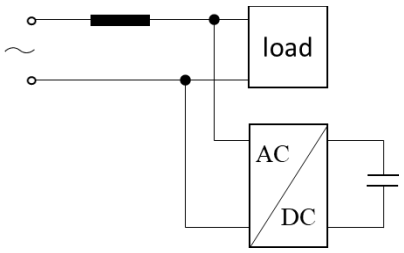
3. Overview of D-suite Technologies

3.1 Classification of D-suite Devices

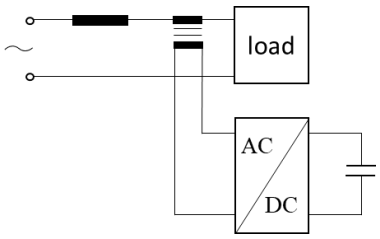
As the LV network is expecting a large uptake of heat pumps, EV chargers and distributed generation, the problems in LV networks will mainly be voltage rise and high circuit and transformer stress due to low carbon technologies. D-suite technologies, which include D-SOPs, D-STATCOMs, D-HFs and D-STs, can mitigate these issues on the LV networks (see Figure 3.1(a)-(d)).



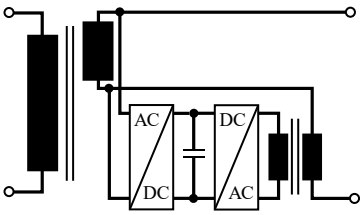
(a) D-SOPs



(b) D-STATCOMs



(c) D-HFs



(d) D-STs

Figure 3.1. Different types of D-suite devices.

The D-SOP is a power electronic interface that has gained significant attention due to its ability to enhance the integration of distributed energy resources (DERs) and improve the overall flexibility and reliability of the grid. D-SOPs are designed to enable active control of power flow and voltage in distribution networks, facilitating the integration of renewable energy sources, energy storage systems, and other DERs.

The D-STATCOM can adopt either a shunt or series configuration to control the system current or voltage by exchanging real and reactive power with the AC system, thereby maintaining the desired voltage level.

The D-HFs are advanced power-quality devices designed to mitigate the detrimental effects of harmonics in distribution networks. When connected in parallel with feeders, D-HFs can actively detect and counteract harmonic currents generated by non-linear loads, such as electronic equipment and variable speed drives, thereby ensuring a clean and stable power supply to connected loads.

The D-ST is a combination of a line-frequency transformer (LFT) with PEDs, which was used to enhance the limited functionalities of the LFT. The D-ST allows the integration of a conventional LFT's high efficiency and low cost with the flexibility of PEDs.

3.2 Modular Design of PEDs in D-suite Devices

3.2.1 Topology selection

The PEDs in the D-Suite devices should be designed with modularity for easy 'plug-and-play'. The basic unit of the PEDs is shown in Figure 3.2, which is a three-phase four-wire converter with the integration of a protection circuit for fault conditions. To facilitate modular design, multiple basic units can be combined to construct different D-Suite devices (i.e., D-STATCOM, D-ST, D-HF and D-SOP). The D-ST and D-SOP require two basic units while the D-STATCOM and D-HF require only one basic unit. For all the D-suite devices, the DC-bus voltage of the PED is selected as 750V, and 1200V Si IGBTs or 1200V SiC MOSFETs can be selected as the semiconductors of the PED.

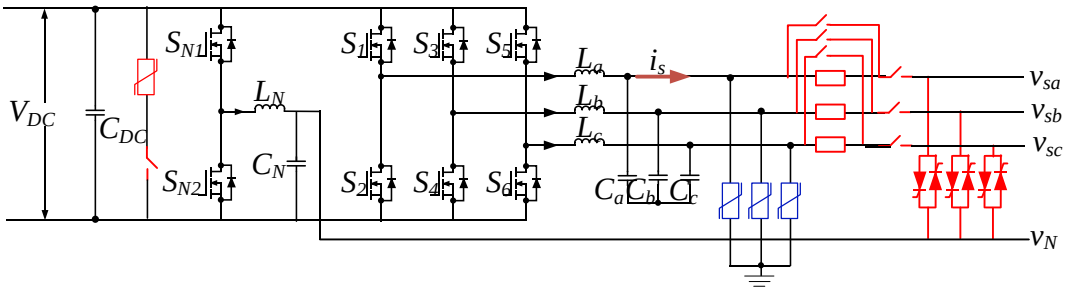
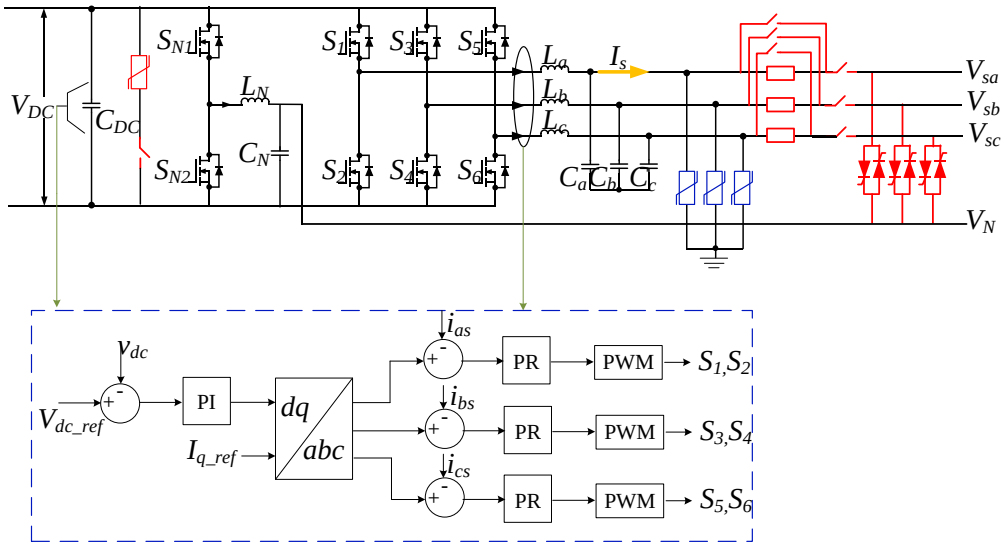


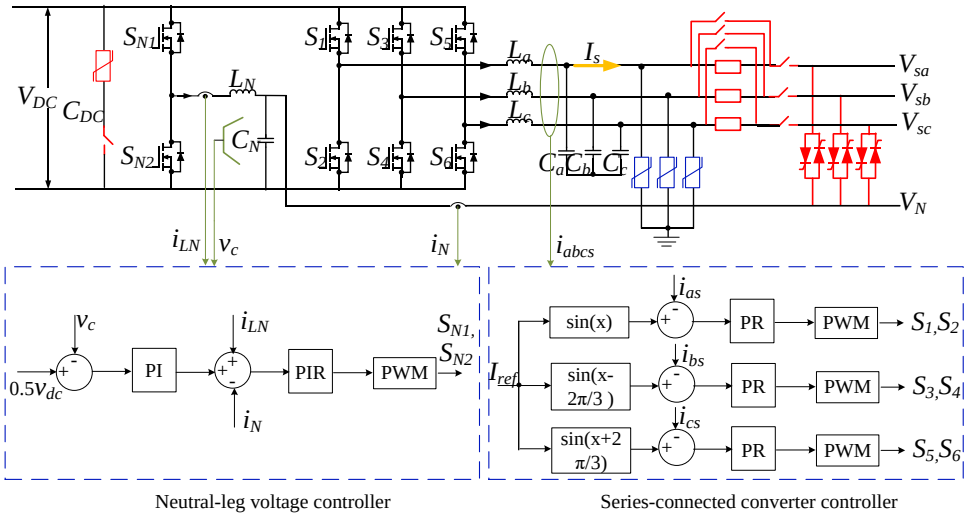
Figure 3.2. The basic unit of PEDs.

3.2.2 Control schematic

In order to examine the utilisation of the D-suite power module, the D-ST has been chosen in this case study. Figure 3.3 depicts the detailed control structures of the back-to-back converter system. This structure comprises two distinct sets of control components: one for the three-phase AC/DC converter and another for the neutral-leg half-bridge converter. The primary distinction in the control mechanisms between the shunt converter and the series converter lies in their respective control modes at the application control level. Specifically, the shunt converter operates in DC voltage and reactive power control modes (see Figure 3.3(a)), while the series converter can operate in independent three single-phase AC current or AC voltage control modes (see Figure 3.3(b)). The neutral leg serves the purpose of providing a pathway for unbalanced current flow. By appropriately managing the neutral leg in Figure 3.3(b), it is possible to effectively mitigate second-order ripples stemming from unbalanced loads on the DC bus. It is noted that only the control strategy of the three-phase converter is depicted in Figure 3.3(a), while the control for the neutral leg is not depicted since it is the same as the Figure 3.3(b).



(a)



(b)

Figure 3.3. Control design of (a) Shunt-connected converter. (b) Series-connected converter.

3.2.3 Simulation Verification

The simulation has been carried out for the H-ST, with the integrated PED having a power rating of 50 kVA at 750 Vdc. Figure 3.4 and Figure 3.5 shows the results for the balanced and unbalanced load current conditions, respectively. In Figure 3.4, the series-connected converter is operating in current control mode, with the three-phase current references are set to be equal to achieve balanced current control. The current is set at 1 p.u to ensure that the converter operates at its fully rated power. The DC link voltage is under the control of the shunt-connected converter and remains at 750 V. Due to the balanced three-phase current control, there is almost no current flowing through the neutral line.

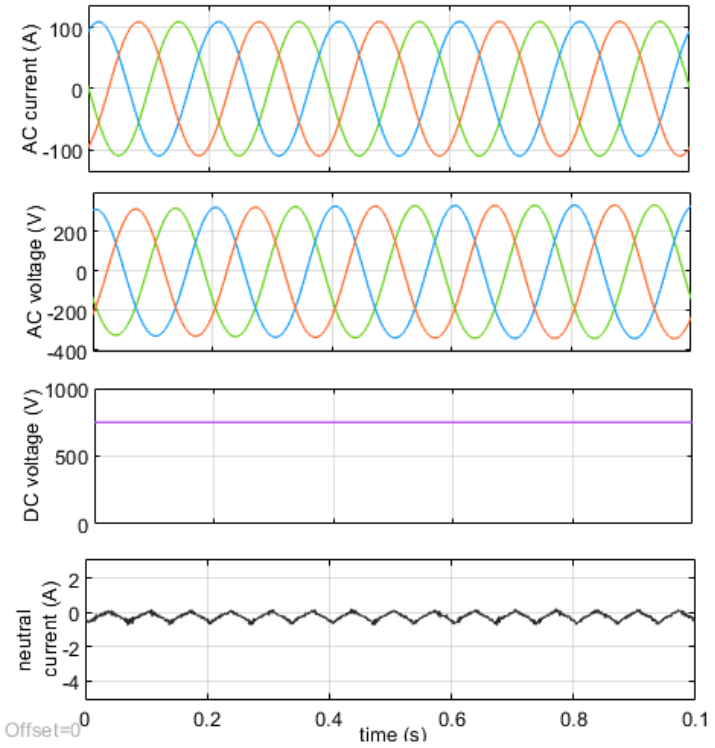


Figure 3.4. Results for series-connected PED under balanced condition. Top: AC current of series converter; Second: AC voltage of series converter; Third: DC link voltage; Bottom: neutral current.

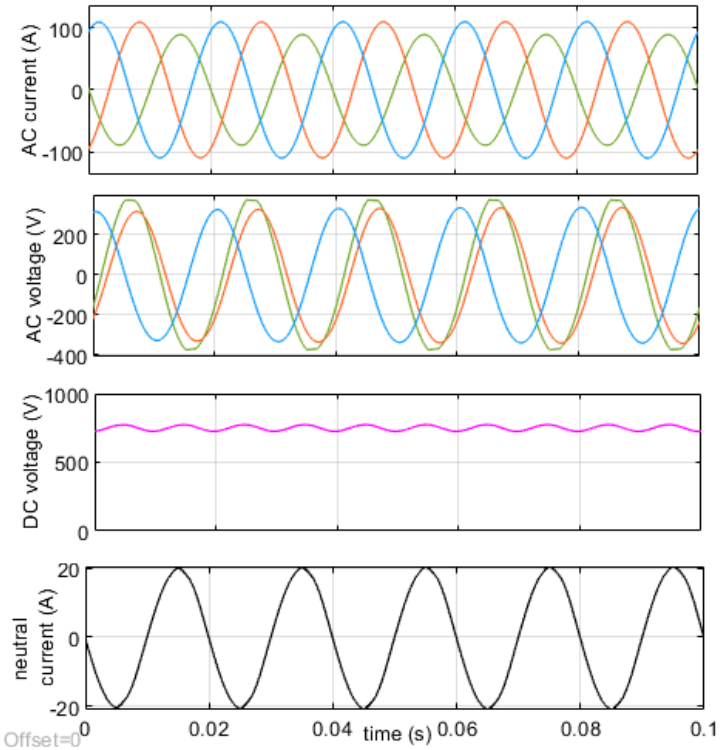
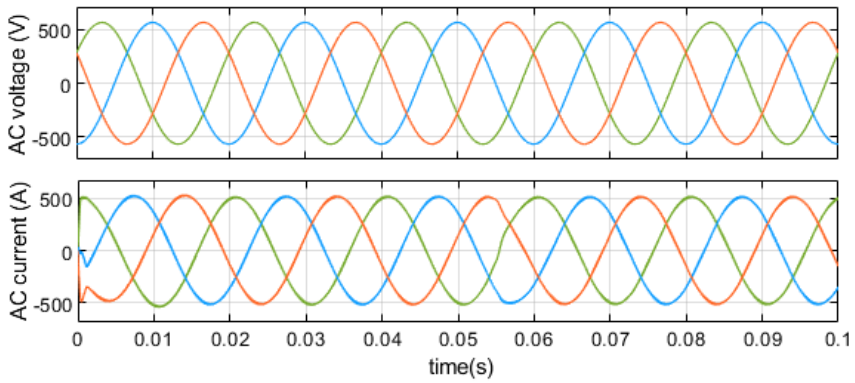
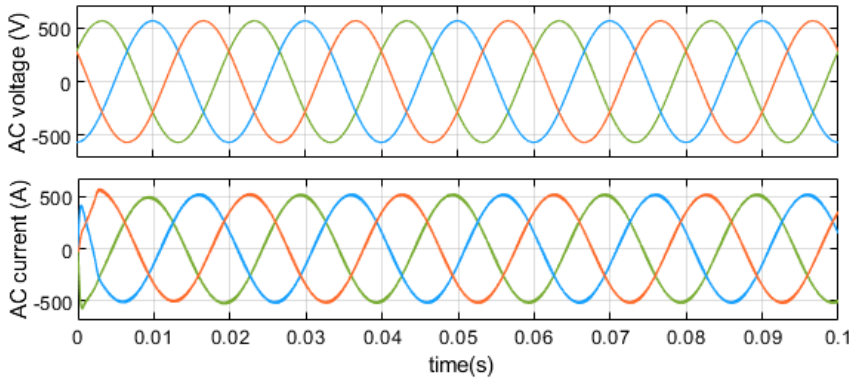


Figure 3.5. Results for series-connected PED under unbalanced condition. Top: AC current of series converter; Second: AC voltage of series converter; Third: DC link voltage; Bottom: neutral current.



(a)



(b)

Figure 3.6. Results for shunt-connected PED under reactive power compensation mode. (a) Capacitive reactive power. (b) Inductive reactive power.

In the event of unbalanced conditions, the three-phase currents are not equal. The current reference in phase A is set as 0.8 p.u while the other two phases maintain a reference of 1 p.u. As illustrated in Figure 3.5, the currents can effectively track their respective references owing to the independent control capability of each phase. Consequently, in this scenario, the DC voltage exhibits a subtle second-order ripple stemming from the unbalanced power distribution. Additionally, due to the unequal currents in the three phases, there is a significant current flowing through the neutral line.

Figure 3.6 illustrates the control of reactive power for the shunt converter. The shunt converter has the capability to supply or absorb reactive power from the grid, thereby enhancing the power factor. In Figure 3.6(a), the converter is operating in a capacitive power control mode, where the current phase leads the voltage by 90 degrees. Conversely, in the inductive power control mode, depicted in Figure 3.6(b), the current lags behind the voltage by 90 degrees.

4. Overview of D-suite technologies

4.1 Multi-objective Optimisation of PED Modules

4.1.1 Trade-offs among cost, power density and efficiency

When selecting switching frequency as the design parameter, there are trade-offs among cost, power density, and efficiency in power electronics systems.

Higher switching frequencies often require the use of more advanced and expensive components, such as high-frequency transformers and fast-switching semiconductor devices. Lower switching frequencies may allow for the use of more cost-effective components but could lead to larger passive components.

In addition, increasing the switching frequency can lead to higher power density by reducing the size of passive components like inductors and capacitors. However, this can also result in increased switching losses, which can generate more power losses and reduce efficiency.

4.1.2 Multi-objective optimisation algorithm

The multi-objective optimisation algorithm is illustrated in Figure 4.1.

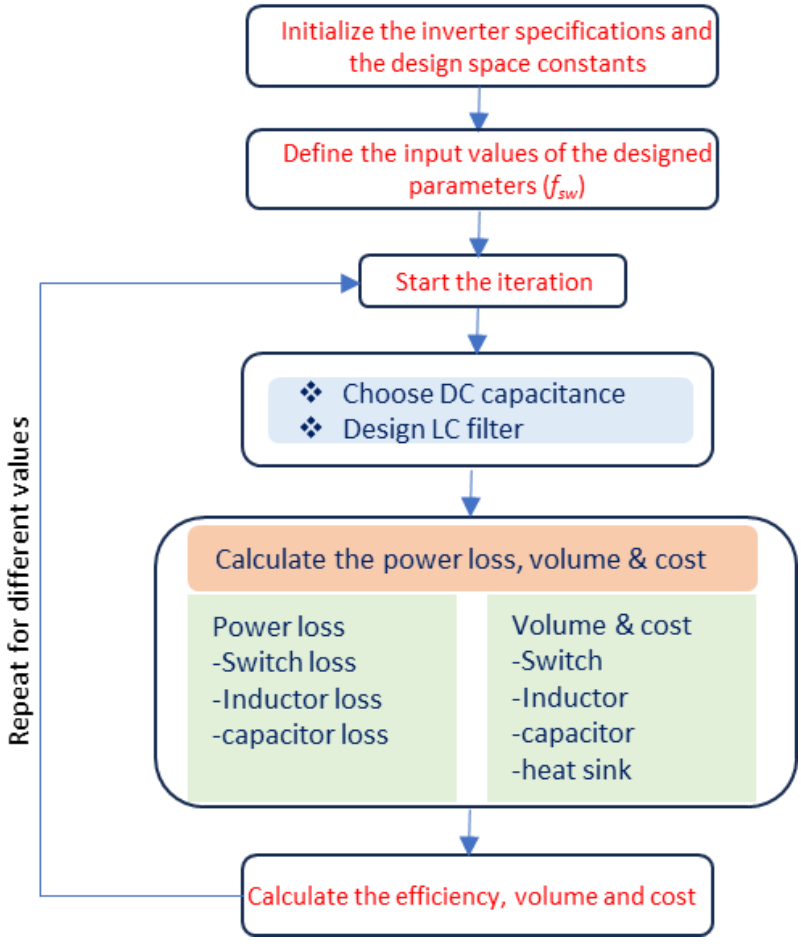


Figure 4.1. Multi-objective optimisation algorithm of PED.

Initially, constant parameters like power rating and thermal impedance are predefined, typically remaining unchanged throughout the design process. In this project, the independent design variable chosen is the switching frequency. To gauge power density, a volume model for passive components must be established. Accordingly, the DC capacitance and LC filter are meticulously designed, taking into account factors such as DC voltage ripple and AC current ripple. In the evaluation of efficiency, comprehensive power loss models for both power semiconductors and passive components are formulated. Consequently, the power density, cost, and efficiency can be determined using these volume and power loss models. The design process is then iterated by selecting different switching frequencies.

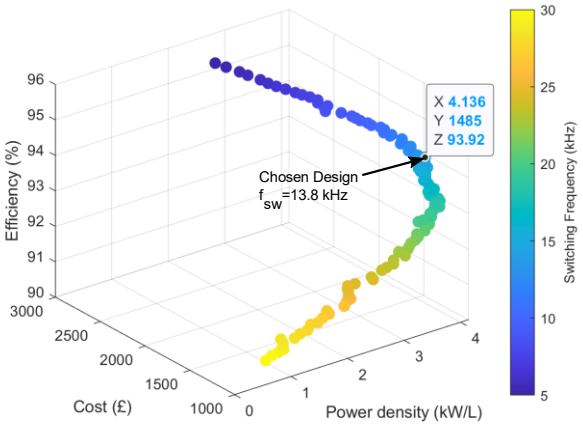


Figure 4.2. Efficiency, Cost and Power density of a 50 kW PED based on Si IGBTs.

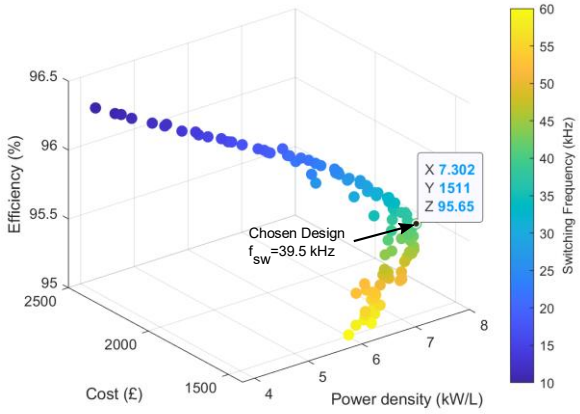


Figure 4.3 Efficiency, Cost and Power density of a 50 kW PED based on SiC MOSFETs.

In this project, the choice between 1200V Si IGBTs and 1200V SiC MOSFETs as semiconductors for the PED is considered. Design optimisation is carried out for both semiconductor types, and the results are presented in Figure 4.2 and Figure 4.3, showcasing simulated efficiency, cost, and power density.

Based on the simulation findings, a switching frequency of 13.8 kHz is selected as the optimal design for the PED when using 1200V Si IGBTs, achieving a maximum power density of 4.1 kW/L. The cost and efficiency of this chosen design are £1,485 and 93.92%, respectively. The total volume of a 50 kW PED is 14.7 L, and the parameters for this selected Si IGBT-based design are summarized in Table 4.1.

On the other hand, when considering 1200V SiC MOSFETs, a different switching frequency of 39.5 kHz is chosen as the optimal design to achieve the maximum power density of 7.35 kW/L. The cost and efficiency for this chosen SiC MOSFET-based design are £1,511 and 95.6%, respectively. The total volume of the 50 kW PED is 6.8 L, and the parameters for this selected SiC MOSFET-based design are summarised in Table 4.2.

Table 4.1 The chosen design parameters of a 50 kW PED based on Si IGBTs.

POWER RATING	50 KW
Maximum series AC voltage (RMS)	230 V
DC-link voltage	750 V
Maximum AC current (RMS)	72.5 A
Switching frequency	14.8 kHz
Switches	1200 V Si IGBTs, IKQ75N120CT2, 2 in parallel
DC capacitance	60 μF
AC filter inductance and capacitance	240 μH, 10 μF
Efficiency	93.9%
Cost (purely power electronics)	£1,485
Power density	4.1 kW/L
Volume	12.1 L

Table 4.2 The chosen design parameters of a 50 kW PED based on SiC MOSFETs.

POWER RATING	50 KW
Maximum series AC voltage (RMS)	230 V
DC-link voltage	750 V
Maximum AC current (RMS)	72.5 A
Switching frequency	39.5 kHz
Switches	1200 V SiC MOSFETs, C3M0016120K, 1 in parallel
DC capacitance	60 μF
AC Filter inductance and capacitance	98.2 μH, 10 μF
Efficiency	95.6%
Cost	£1,511
Power density	7.35 kW/L
Volume	6.8 L

It's worth noting that the PED based on SiC MOSFETs outperforms the Si IGBT-based PED, achieving higher power density and efficiency. However, the SiC-based PED comes at a slightly higher cost due to the expensive nature of SiC MOSFETs. Nonetheless, the choice of the SiC-based PED is justified in this project due to its superior power density, aligning with the project's objectives.

4.2 Protection Design of PED Modules

4.2.1 Overview of the protection requirements in LV networks

Grid faults can be categorised into two distinct groups, which are overcurrent faults and overvoltage faults (see Figure4.1). Overcurrent faults primarily arise from grid overloads and short circuits, with durations ranging from seconds to minutes. It's important to note that short circuits impose significantly higher current stresses on the D-ST compared to overloads. Additionally, when the D-ST system is connected to the grid, inrush currents can occur.

On the other hand, overvoltage faults, such as lightning and switching surges, are primarily caused by phenomena like lightning impulses (LIs) and switching impulses (SIs). These surges typically last for durations spanning from a few tens of microseconds to a few milliseconds. In contrast, temporary line-frequency overvoltage faults can endure for up to hours and are primarily triggered by earth faults. It's worth noting that temporary faults are generally considered less critical in comparison to lightning and switching surges.

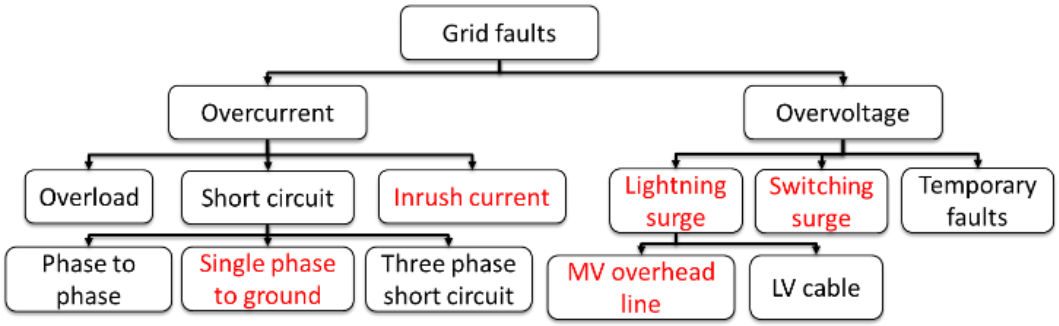


Figure 4.1. Classification of grid faults.

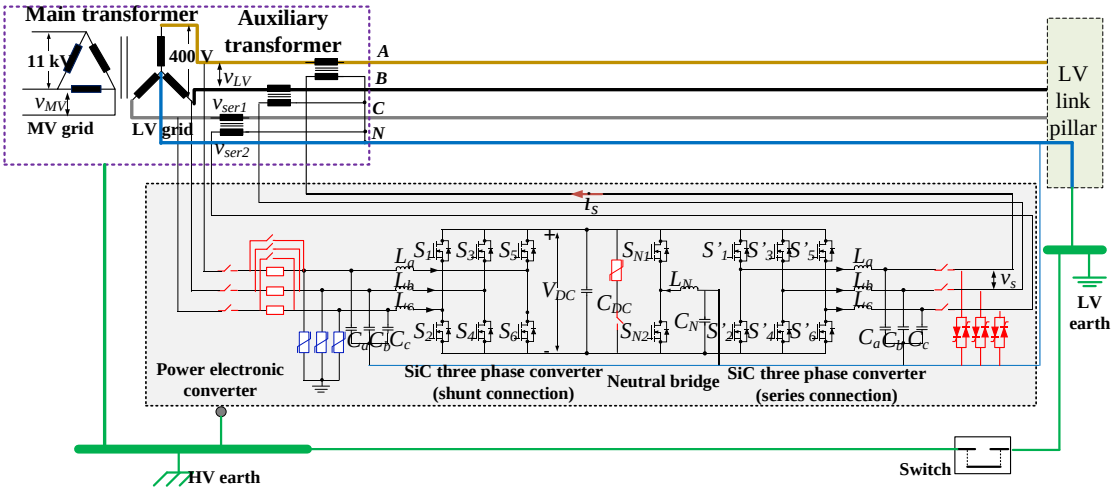


Figure 4.2. The D-ST topology with all overcurrent and overvoltage protection circuits.

In Figure 4.2, the schematic of the D-ST including all the designed overcurrent and overvoltage protection circuits is presented. Overcurrent protection is achieved through the use of bypass thyristors and a pre-charging circuit, while overvoltage protection is implemented by

incorporating DC-link clamping circuitry and varistors. The detailed description of protection methods is given in the following sections.

4.2.2 Protection design of the D-ST under overcurrent faults

In the event of phase-to-ground short circuit fault, the grid overcurrent would arise. The converter would be overloaded and damaged if being without proper protection. To this end, a set of anti-parallel thyristors are used for bypassing the converter under the short circuit fault. As seen the Figure 4.2, these thyristors are connected to the AC side of the series converter at the secondary transformer.

Figure 4.3 shows the simulation results for the protection of the phase-to-ground short circuit fault. At the beginning, the converter is operated under the normal conditions. At the time 1 s, the short circuit fault occurs and the fault current rise up to around The fault is detected by the fault detection measures and the bypass thyristors are closed so that the fault current would not flow through the converter (Due to the very fast fault detection, the overcurrent detection time is omitted). The fault lasts for 2 seconds until the AC circuit breaker is opened. During the period of protection, the thyristor junction temperature increases to 120 ℃, which is below the maximum temperature (i.e., 150 ℃).

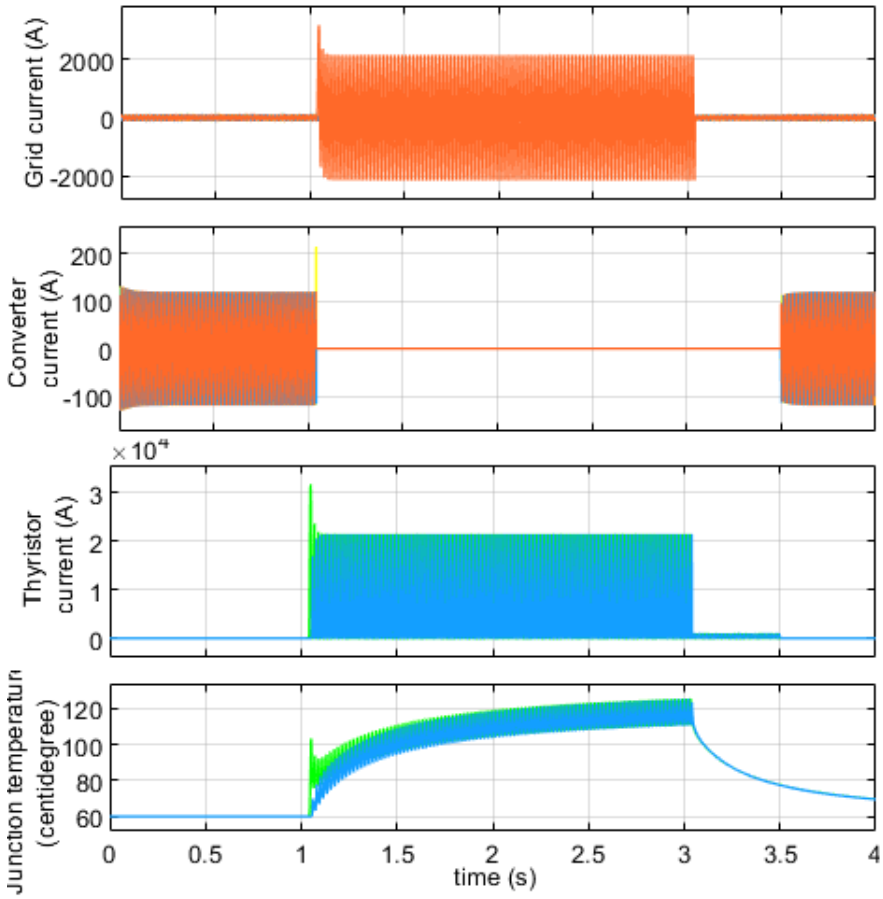


Figure 4.3. Simulation for a phase-to-ground short circuit.

On the other hand, the high inrush current may occur if the pre-charging resistor is not implemented. Since the initial-state voltage of the dc capacitor is zero, there may induce an instantaneous large AC current when the circuit breaker is closed. Figure 4.4 shows the inrush

current without using pre-charging resistor. As can be seen, the current peak rise up to more than 200 A at the instance of closing the circuit breaker. The high inrush current charges the DC voltage to around 1100 V through the anti-parallel diode.

To mitigate the inrush current, the pre-charging resistor is used (highlighted with red colour in Figure 4.2). The pre-charging resistor limits the inrush current below 50 A, which is shown in Figure 4.5. Since the peak current is highly mitigated, the DC voltage is charged to around 600 V, which is lower than the DC voltage in Figure 4.4.

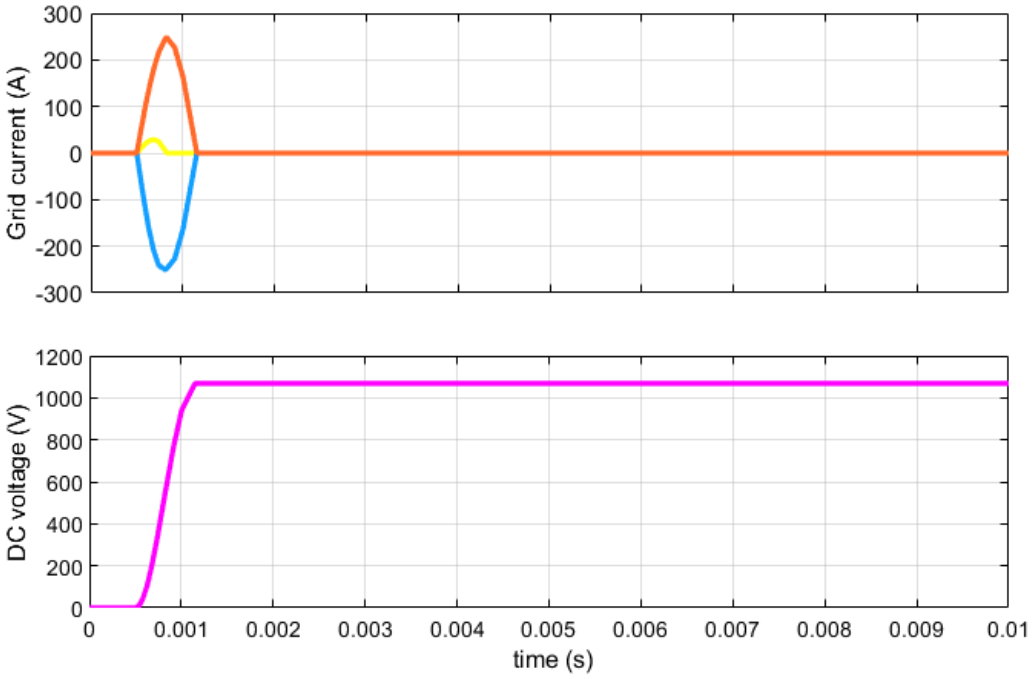


Figure 4.4. Simulation for inrush current without pre-charging circuit.

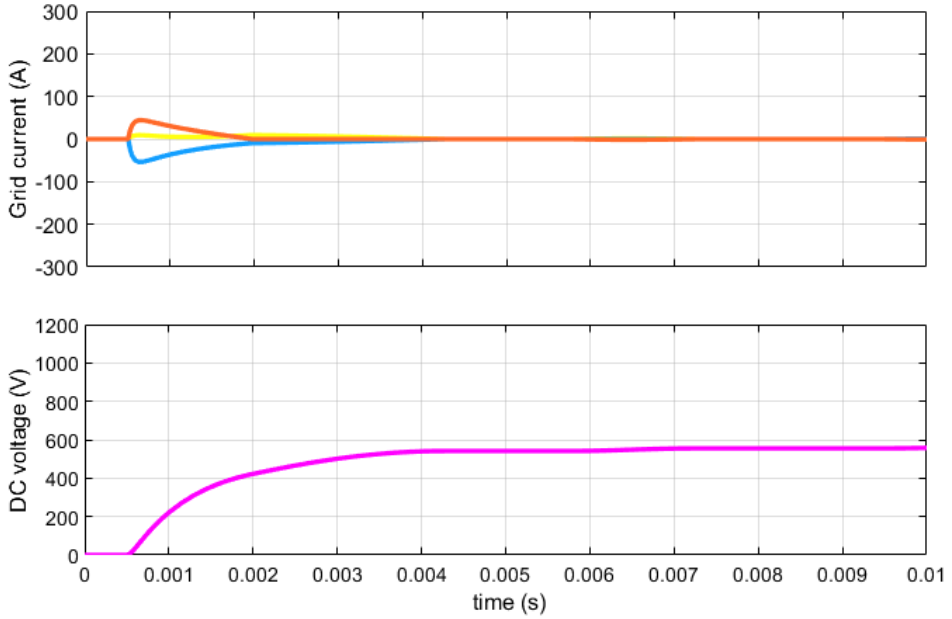


Figure 4.5. Simulation for inrush current with pre-charging circuit.

4.2.3 Protection design of the D-ST under overvoltage faults

To protect the lightning surge, the varistors are connected between three phases of the shunt converter and ground. Figure 4.6 and Figure 4.7 display the simulation results of the 1.2/50-μs, 110-kV lightning impulse test.

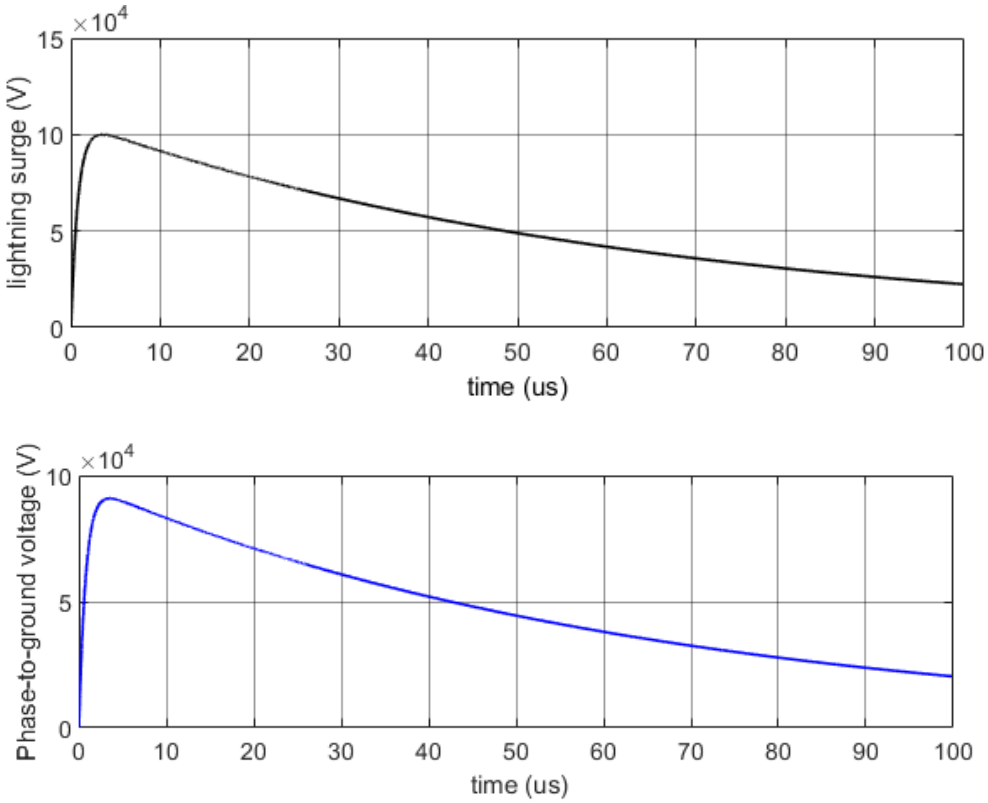
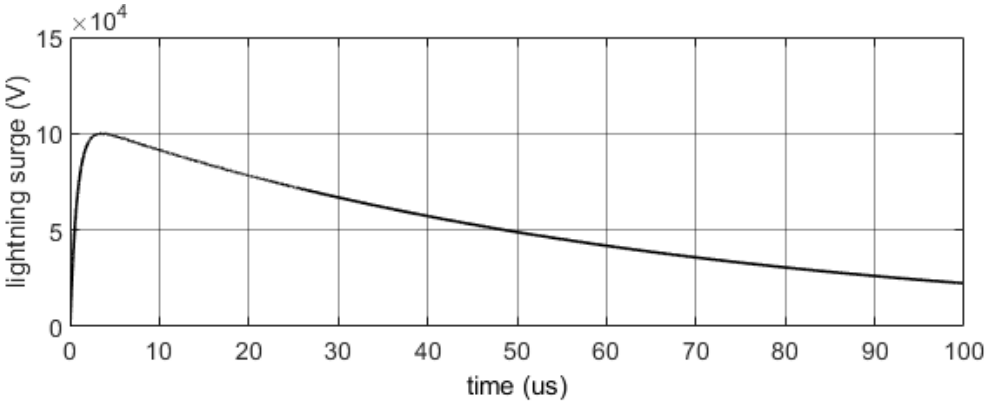


Figure 4.6. Simulation for lightning surges without varistors.



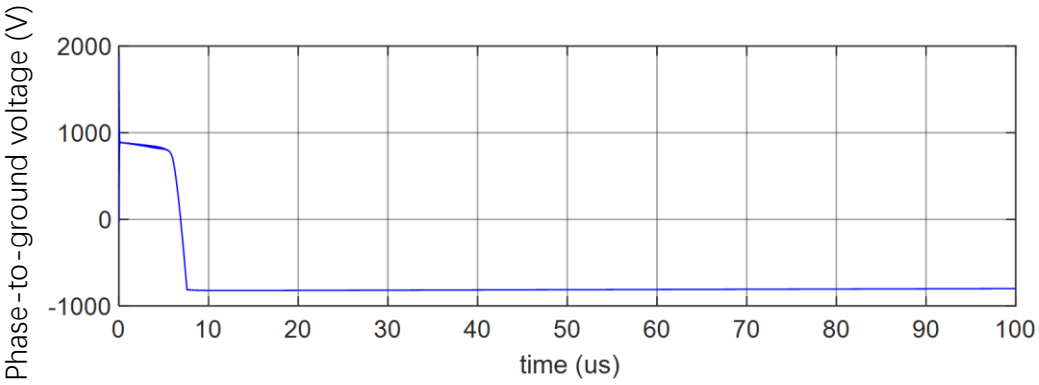


Figure 4.7. Simulation for lightning surges with varistors.

In Figure 4.6, the simulation was performed in the absence of varistors within the circuit. This led to the propagation of the lightning surge from the MV side to the converter, resulting in an excessive overvoltage exceeding 90 kV for the converter-side phase-to-ground voltage. Conversely, in Figure 4.7, the installation of varistors at the input of the shunt converter effectively constrained the converter-side phase-to-ground voltage below 1000 V.

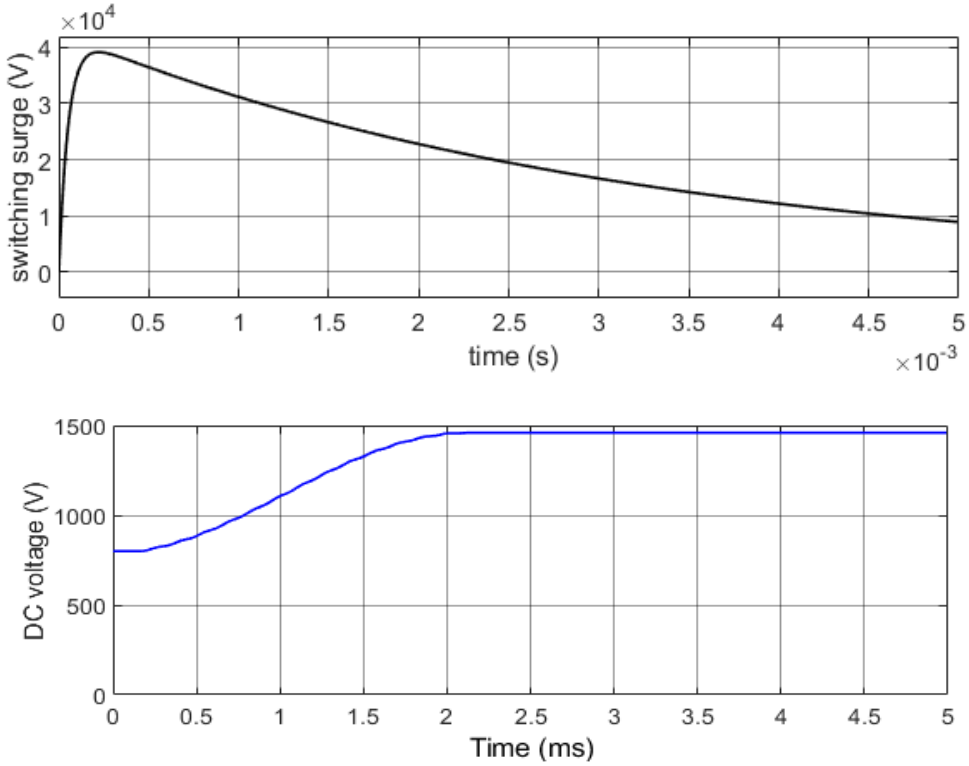


Figure 4.8. Simulation for switching surges without DC clamping circuits.

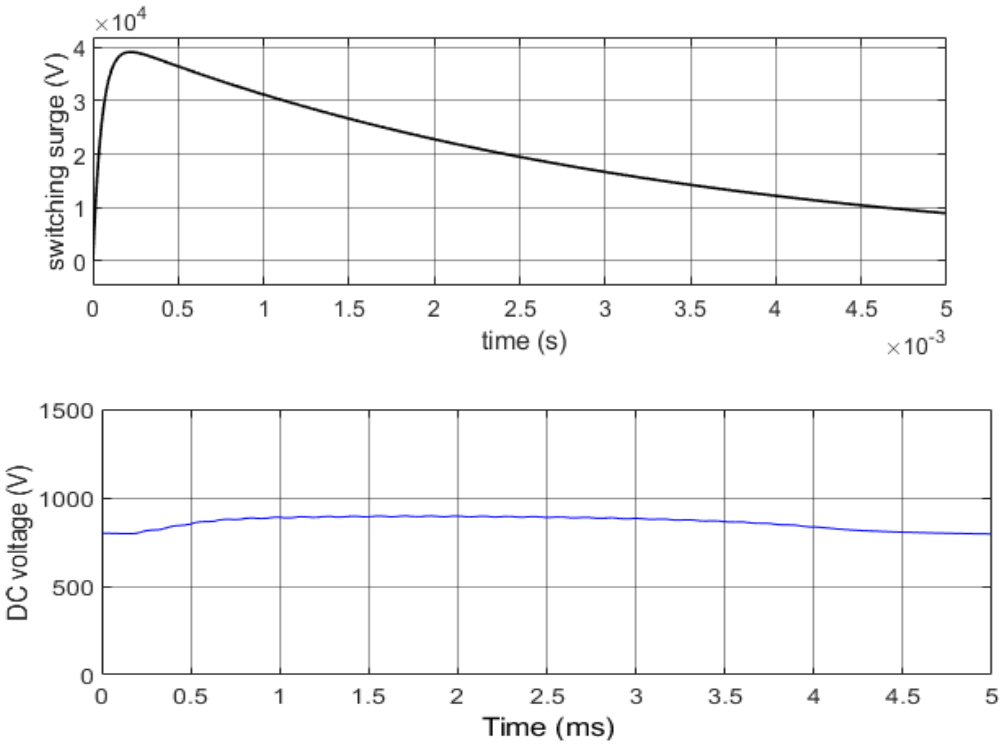


Figure 4.9. Simulation for switching surges with DC clamping circuits.

In order to explore the effects of the switching surge, a 250/2500-μs, 38.9-kV switching impulse is introduced between two MV terminals of the D-ST system. The impulse transfers a substantial amount of energy to the converter's DC-link, leading to a notable increase in voltage on the DC-link. Consequently, a DC-link clamping circuit is employed to restrict the DC-link voltage within an appropriate range.

Simulation verification was employed to assess the effectiveness of switching surge protection. Figure 4.8 and Figure 4.9 illustrate the simulated surge voltage and the dc-link voltage. In Figure 4.8, the simulation was executed without the inclusion of a dc-link clamping circuit within the circuit. This omission results in the switching surge causing the dc-link voltage to surge to 1450 V. Subsequently, a DC-link clamping circuit is introduced into the simulation model, as shown in Figure 4.9. This clamping circuit constrains the dc-link voltage to a maximum of 900 V.

5. Conclusions

In conclusion, this report provides an extensive overview of D-suite technologies, their modular design, control schematics, and simulation verification, focusing on the context of LV networks facing challenges related to the adoption of heat pumps, EV chargers, and distributed generation. The D-suite devices, including D-SOPs, D-STATCOMs, D-HFs, and D-STs, are introduced as solutions to mitigate voltage rise and high circuit and transformer stress resulting from the integration of LCTs.

Below are the key outcomes from the report:

- Modular Design of PEDs: The modular design of PEDs within D-suite devices enables a "plug-and-play" approach, making it possible to construct different D-Suite devices by combining multiple basic units. This modular approach allows for flexibility and scalability in designing solutions for LV networks.
- Multi-objective Optimisation: Designing D-Suite devices involves optimising parameters such as switching frequency, which requires considering trade-offs among cost, power density, and efficiency. Higher switching frequencies offer benefits like reduced passive component size but may require more advanced and expensive components. Careful consideration is essential to strike the right balance.
- Protection Requirements: To ensure the reliability of D-Suite devices in LV networks, comprehensive protection measures are developed and implemented. Overcurrent protection involves the use of bypass thyristors and pre-charging circuits to safeguard against short circuits and inrush currents. Overvoltage protection includes the use of varistors and DC-link clamping circuits to protect against lightning and switching surges.
- Simulation Verification: The effectiveness of control and protection measures have been confirmed through simulation verification. Simulations demonstrate the power flow control enabled by the integrated PED and how protection circuits effectively limit overvoltage and overcurrent, ensuring the safety and reliability of D-Suite devices.

Overall, the report provides a comprehensive understanding of D-Suite technologies, their design considerations, and the importance of protection mechanisms, emphasising the critical role these solutions play in addressing the challenges associated with the adoption of low-carbon technologies in LV networks.

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