SP Energy Networks

D-Suite

Protection and integration of D-Suite devices

ABOUT REPORT

Report Title	Protection and Integration of D-Suite Devices
Report Status	Final
Project Reference	D - Suite

REPORT PROGRESS

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VERSION HISTORY

Date	Issue	Status
08/03/2024	1.0	Final Version
21/03/2024	1.1	Branding updated for sharing on the SNP.

Index

1. Abbreviations

Abbreviation	Term
D-ST	D-Suite Smart Transformers
LV	Low Voltage
LI	Lightning Impulse
LFT	Line-Frequency Transformer
MV	Medium Voltage
PED	Power Electronic Device
SI	Switching Impulse

2. Executive Summary

This report focuses on D-Suite Smart Transformers (D-ST) as a proposed Power Electronic Device (PED) solution, consisting of a slim line-frequency transformer (LFT) integrated with the PED. Unlike traditional LFTs, D-STs offer enhanced flexibility, including power flow control, voltage regulation, and load balancing capabilities. The report primarily addresses practical development requirements, focusing on protection measures and dimension estimation for D-STs.

Protection requirements are established to safeguard D-STs during fault occurrences, categorised into external grid faults and internal PED faults. External grid faults necessitate protection measures to withstand overcurrent and overvoltage events, while internal faults demand failsafe PED operation to ensure uninterrupted transformer functionality.

Key findings of the report include:

- Overview of protection requirements for a D-ST (500 kVA, 11 kV/400 V transformer with 50 kVA PED) across various fault scenarios, emphasising critical external grid faults like phase-to-ground short circuits, converter inrush currents, lightning surges, and voltage surges. Internal PED faults require swift and accurate fault detection for immediate disconnection from the grid, allowing the LFT to maintain power transfer between medium and low-voltage grids.
- Development of protection mechanisms tailored to shield the PED during critical external grid faults. These mechanisms include bypass thyristors for short-circuit protection, pre-charging circuits to limit converter inrush currents, and varistors along with DC-link clamping circuits for lightning and switching surge protection.
- Presentation of a 3D rendering of the D-ST based on optimised design outcomes from previous work packages. The estimated dimensions of the D-ST are 2.20m Length × 1.10m Width × 1.58m Height.
- Highlighting the compact dimensions of the PED and the additional series-connected transformer, which are 1.2% and 11% of the main transformer's dimensions, respectively, facilitating seamless integration.
- Emphasis on the need for future protection developments to ensure intrinsic fail-safe operation of D-STs, especially in cases of protection mechanism failures. The ultimate goal is to design and manufacture intrinsically safe D-STs without compromising voltage supply provision through the main transformer.
- This report underscores the significance of protection measures and optimised dimensions in realising the full potential of D-ST as efficient and reliable PED solutions.
- The D-ST configuration is composed of two fundamental D-Suite modules, enabling the application of the presented protection methods to other types of D-Suite devices. These devices are constructed by interconnecting basic D-Suite modules in various configurations. This modular approach facilitates flexibility and scalability in implementing protection measures across different D-Suite device configurations, ensuring adaptability to diverse operational requirements and system configurations.

3. Overview of the Protection Requirements

Protection requirements for the D-ST have yet to be defined in standards. Therefore, this section provides an overview of protection requirements based on potential realistic fault scenarios and, where applicable, draws from standards for conventional power transformers such as IEC 60076.

A range of fault scenarios may occur in PEDs operating within distribution grids. Broadly, these scenarios can be categorised into external faults originating from the grid, imposing stresses on the PED, and internal faults occurring within the PED.

Grid faults can be classified into two main categories, as illustrated in

Figure 1. Overcurrent faults, typically arise from grid overloads or short circuits, lasting for seconds or minutes. Short circuits, subject the D-ST to significantly higher current stresses compared to overloads. Additionally, inrush currents could occur when the D-ST connects to the grid. On the other hand, overvoltage faults, including lightning and switching surges, stem from lightning impulses (LIs) and switching impulses (SIs) with typical durations ranging from a few tens of microseconds to milliseconds. Furthermore, temporary line-frequency overvoltage faults, persisting for up to hours, are predominantly caused by earth faults. These temporary faults are generally considered less critical than lightning and switching surges.

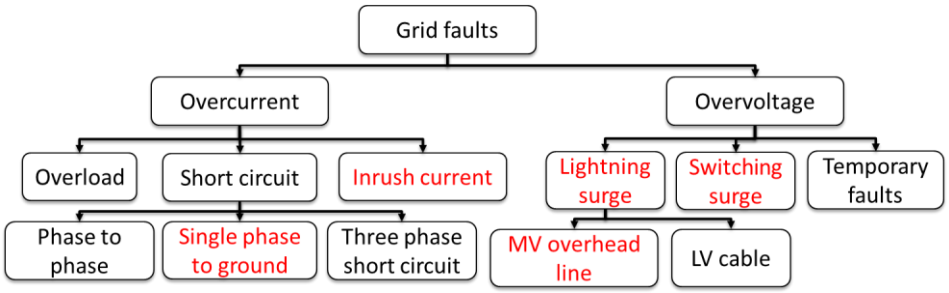


Figure 1 Classification of grid faults.

4. Protection Design of the D-ST During Overcurrent Faults

Models have been developed to analyse the impacts of the most critical faults on the PED. These models are instrumental in assessing the effectiveness of the designed protection mechanisms. Each fault needs a dedicated simulation model due to variations in timescale and the related components of the system.

4.1 Protection Design of Phase-to-ground Short Circuit

To analyse the protection, against phase-to-ground short circuits, we utilise the simulation model depicted in Figure 2. Given the extended fault duration of 2 seconds, parasitic capacitances are omitted, allowing the LFT to be represented by its short-circuit impedance Z_{sc}. Additionally, the grid impedance minimally impacts the short-circuit current in the LV grid, particularly in the worst-case scenario, where the short circuit arises near the LV winding terminals of the LFT.

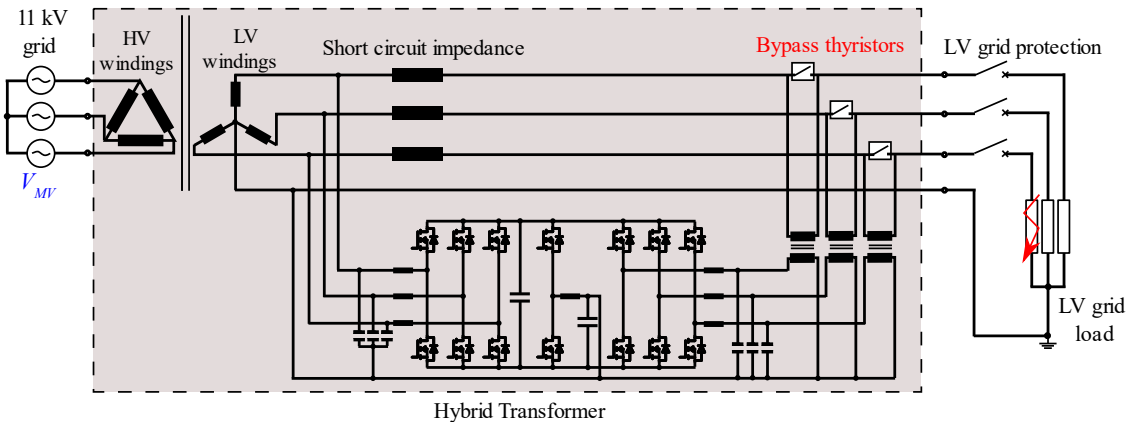


Figure 2 Model for single-phase-to-ground short circuit.

Table 1 The optimised design parameters of a 50 kW PED in the selected D-ST.

Power rating	50 kW
Maximum series AC voltage (RMS)	230 V
DC-link voltage	750 V
Maximum AC current (RMS)	72.5 A
Switching frequency	39.5 kHz
Switches	1200 V SiC MOSFETs, C3M0016120K, 1 in parallel
DC capacitance	60 μF
AC Filter inductance and capacitance	98.2 μH, 10 μF
Efficiency	95.6%
Cost	[redacted]
Power density	7.35 kW/L
Volume	6.8 L

The PED parameters are modelled based on the optimised design results obtained from previous work packages, as outlined in Table 1. Grid short circuits are investigated under full load conditions of the PED. Given the high current amplitude and a fault duration of 2 seconds, conducting the fault current, solely through the PED, would need significant overrating. A more practical approach involves incorporating bypass switches to divert the current away from the PED during fault conditions. To prevent excessive stresses on inductors and semiconductors, the PED is promptly turned off, and the bypass switches are activated upon detecting an overcurrent.

Thyristors are selected as the bypass switches for PED protection, ensuring a rapid closing time ($t_{bypass} \leq 100\ \mu s$) to minimise voltage and current stresses. Fault detection is triggered by hardware comparators, which operate much faster than the bypass thyristor closing time, allowing detection time to be disregarded. The proposed bypass switch configuration comprises four thyristors per phase, as illustrated in Figure 3. Thyristors A and B are connected in parallel to handle high-amplitude fault currents, while Thyristors C and D are also parallel but anti-parallel to A and B, facilitating alternative current flow. Each thyristor is designed to carry an RMS current of

$$I_{Thy} = \frac{I_{sc,rms}}{4} = 3.8\ \text{kA}.$$

To accommodate this current rating, four press-pack 200 V, 7.95 kA thyristors, model T3710N by Infineon, are utilised on each phase. The parameters of these thyristors are detailed in

Table 2. Additionally, the thermal impedance model of the thyristors, obtained from the datasheet, is incorporated into the simulation model to simulate the junction temperature of the thyristors during the fault event. It is crucial to ensure that the thyristors can conduct the fault current for 2 seconds without surpassing their maximum junction temperature (withstand capability).

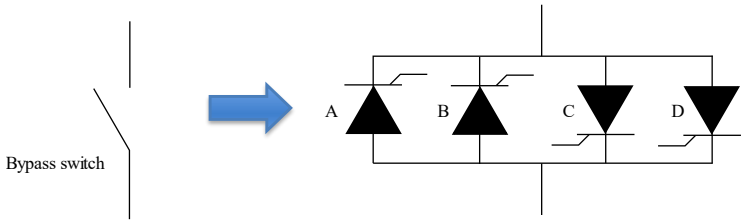


Figure 3 Thyristors for the bypass switch per phase.

Table 2 Parameters of the thyristor bypass switch.

	Parameters
Thyristors	Infineon T3710N, 200 V, 7.95 kA, 4 per phase
Package	Press packs
Gate driver	Pulsed and linear current sources
Turn-on delay	4 μs
Maximum junction temperature	140 °C

4.2 Protection Design of Converter Inrush Current

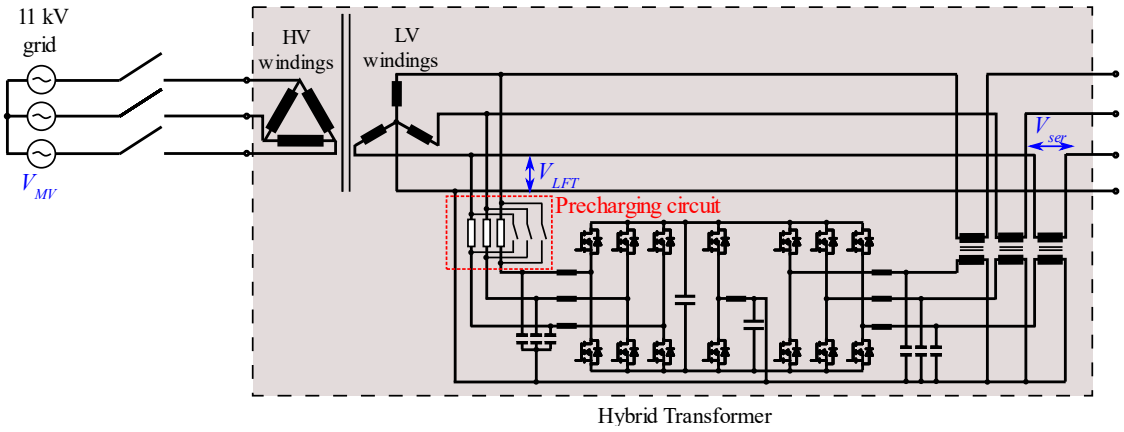


Figure 4 Model for converter inrush current.

To analyse the protection against converter inrush current, we employ the model depicted in Figure 4. Initially, the D-ST is at no load upon connection to the 11 kV MV grid. The semiconductors in the PED remain inactive, functioning as a diode rectifier, to incrementally charge the DC link from 0 V to its nominal operational voltage. Upon connection to the 11 kV grid, the low impedance of the PED triggers a substantial inrush current.

To mitigate this inrush current, a pre-charging circuit is designed to constrain its amplitude within the current rating of the PED. The pre-charging circuit, outlined in the red dashed box in Figure 4, comprises three pre-charging resistors and bypass switches. Upon connection to the 11 kV grid, the bypass switches in the pre-charging circuit remain open, allowing the DC link of the PED to charge through the pre-charging resistors. This limits the amplitude of the inrush current. Once the DC-link voltage reaches its full charge, the bypass switches are closed, excluding the pre-charging resistors from normal PED operation to minimize losses. The pre-charging resistors are chosen to have a resistance of 5 Ω to ensure that the inrush current amplitude remains below 50 A.

5. Protection Design of the D-ST Under Overvoltage Faults

In this section, we focus on the investigation of overvoltage faults induced by lightning surges and switching surges. A suitable protection circuit is designed to mitigate the effects of these overvoltage faults. Notably, the impulse withstands requirement for partial discharges is not factored into this analysis, as it predominantly depends on cables and transformers rather than the PED. However, this requirement needs to be considered in future when designing and selecting cables and transformers.

5.1 Protection Design of Lightning Surge

In the event of lightning transients, accounting for the parasitic capacitances of the transformer becomes imperative as they profoundly affect the propagation of rapid voltage transients to the back-to-back converter. To address this, a simplified high-frequency model of the LFT is employed[1], prioritising the transmission of the voltage pulse to the converter over internal voltage distribution across the winding. These couplings are integrated into the low-frequency model, which encompasses leakage and magnetising inductance, resulting in the formation of the single-phase two-winding model depicted in Figure 5. The primary parasitic capacitances are listed in

Table 3, sourced from [2]. It is assumed that these parasitic capacitances are identical across all phases, with negligible inter-phase couplings. Consequently, a three-phase model can be derived by connecting the terminals of the single-phase models in either a delta or star configuration.

Figure 6 depicts the complete model including the LFT, PED, and its filter elements. Furthermore, varistors are applied at the input of the shunt converter for overvoltage protection. The PED is switched off during the lightning test.

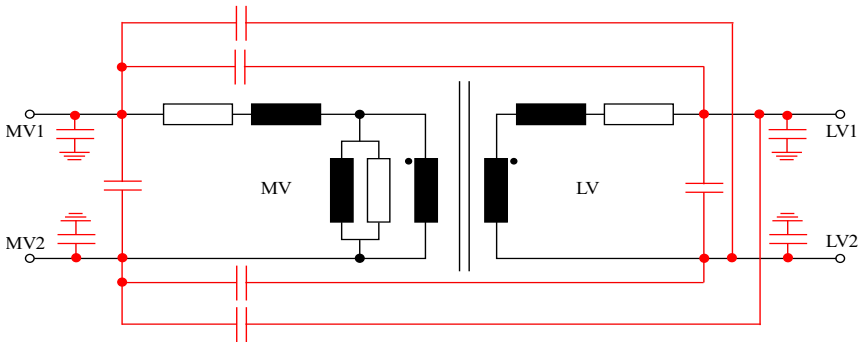


Figure 5 Single-phase high-frequency transformer equivalent circuit model.

Table 3 Parasitic capacitances of the high-frequency transformer equivalent circuit model.

[1] J. Burkard and J. Biela, “Protection of hybrid transformers in the distribution grid,” in Proc. 18th Eur. Conf. Power Electron. Appl., 2016, pp. 1–10.
[2] J. Burkard and J. Biela, "Design of a Protection Concept for a 100-kVA Hybrid Transformer," in IEEE Transactions on Power Electronics, vol. 35, no. 4, pp. 3543-3557, April 2020.

Parameter	Value
$C_{MV1-LV1}$, $C_{MV2-LV1}$, $C_{MV1-LV2}$, $C_{MV2-LV2}$	144 pF
$C_{MV1-GND}$, $C_{MV2-GND}$, $C_{LV1-GND}$, $C_{LV2-GND}$	87 pF
$C_{MV1-MV2}$, $C_{LV1-LV2}$	72 pF

Due to the extremely low time constants associated with the considered 1.2/50 µs, 110 kV lightning impulse, and its common mode nature, the magnetic coupling of the LFT can be negligible for this scenario. However, the parasitic capacitances of the transformer play a significant role in providing high-frequency coupling between the MV and LV windings, as well as with the ground.

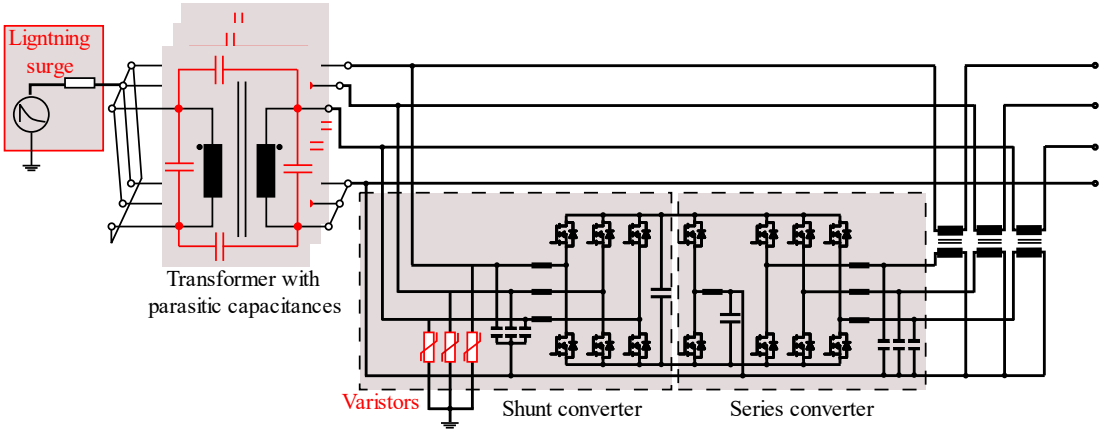


Figure 6 Model to study the propagation of common mode lightning surges from the MV side to the PED (Note: the capacitors highlighted in red represent parasitic capacitors inherent to the 11kV to 400V transformers, rather than capacitors added externally).

To protect the converter against excessive phase-to-ground overvoltage, varistors (such as the Littelfuse LST2755VL2NT1, with a clamping voltage of 900 V) are installed between each phase of the shunt converter and ground. These varistors serve as protective devices, dissipating excess energy and limiting the voltage spikes experienced by the converter during transient events.

5.2 Protection design of switching surge

The model for investigating the effects of 250/2500 µs switching impulses is illustrated in Figure 7. In this scenario, transients in the millisecond range are induced. Consequently, the capacitive couplings of the LFT play a minor role, while magnetic couplings become predominant. A 250/2500 μs, 38.9 kV switching impulse is applied between two MV terminals of the D-ST within the model. Additionally, the model includes a DC-link clamping circuit for overvoltage protection.

The considered 250/2500 µs, 38.9 kV switching impulse transfers a substantial amount of energy to the DC-link of the converter through the magnetic coupling of the LFT. This leads to a significant voltage rise on the DC-link, which must be controlled to prevent semiconductor breakdown. To address this, a DC-link clamping circuit is implemented to limit the voltage rise within safe levels.

Varistors with a clamping voltage of 900 V (such as the Littelfuse LST2755VL2NT1) are selected for the DC-link clamping circuit. However, to prevent overheating of the varistors under nominal DC-link voltage conditions, they are connected in series with an IGBT (such as

the Infineon IKQ75N120CT2, rated at 1200 V, 150 A, with 2 in parallel) controlled by a hysteresis logic. This arrangement ensures effective voltage clamping while maintaining the operational safety and reliability of the converter system.

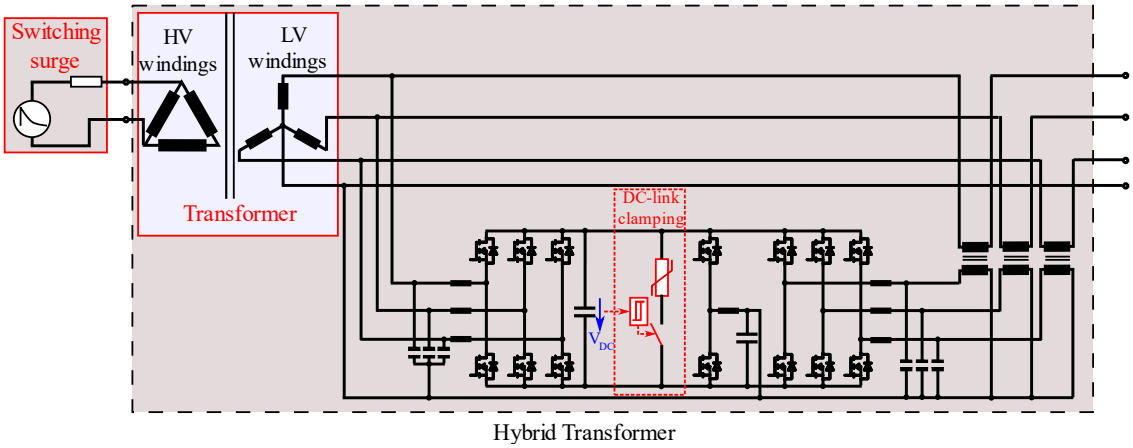


Figure 7 Model to study the overvoltage induced by the MV-side switching surge.

In Figure 8, the schematic of the D-ST is depicted, showcasing all the designed overcurrent and overvoltage protection circuits. The overcurrent protection circuits, including the bypass thyristors and pre-charging circuit, are highlighted in red. Conversely, the overvoltage protection circuits, comprising the DC-link clamping circuit and varistors, are highlighted in blue. This colour-coded representation aids in visualising the distinct protection mechanisms employed to protect the D-ST against potential fault conditions.

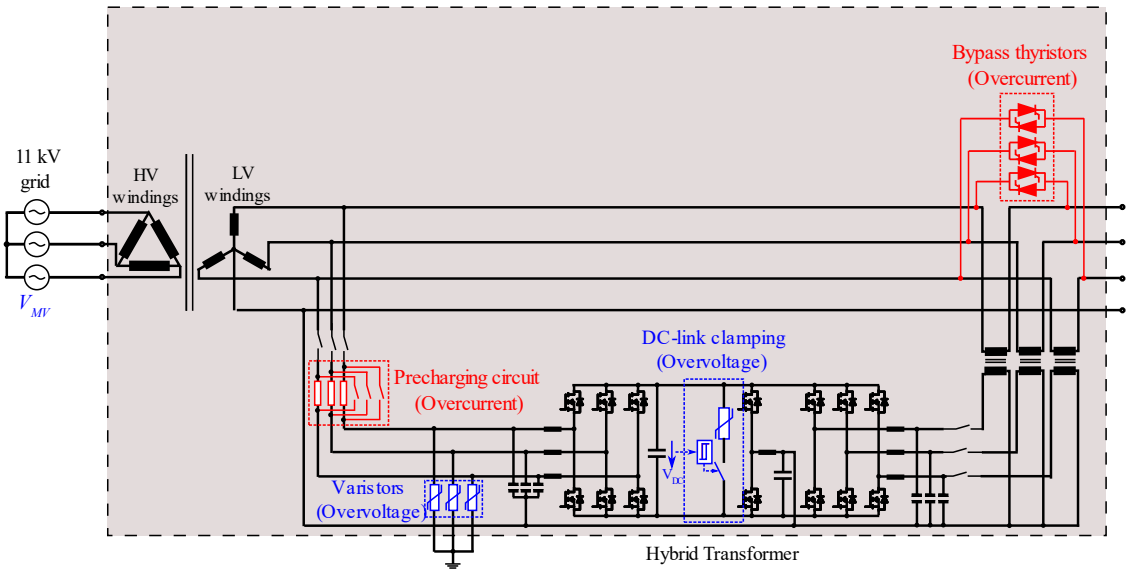
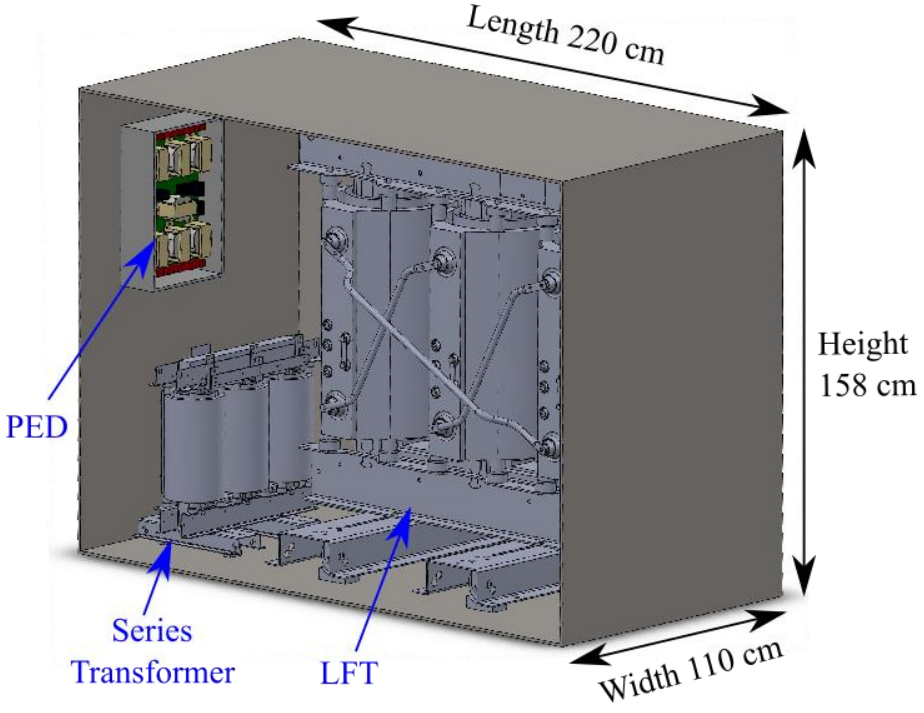


Figure 8 The D-ST topology with all designed overcurrent and overvoltage protection circuits.

6. 3-D rendering and the estimated dimension of the D-ST

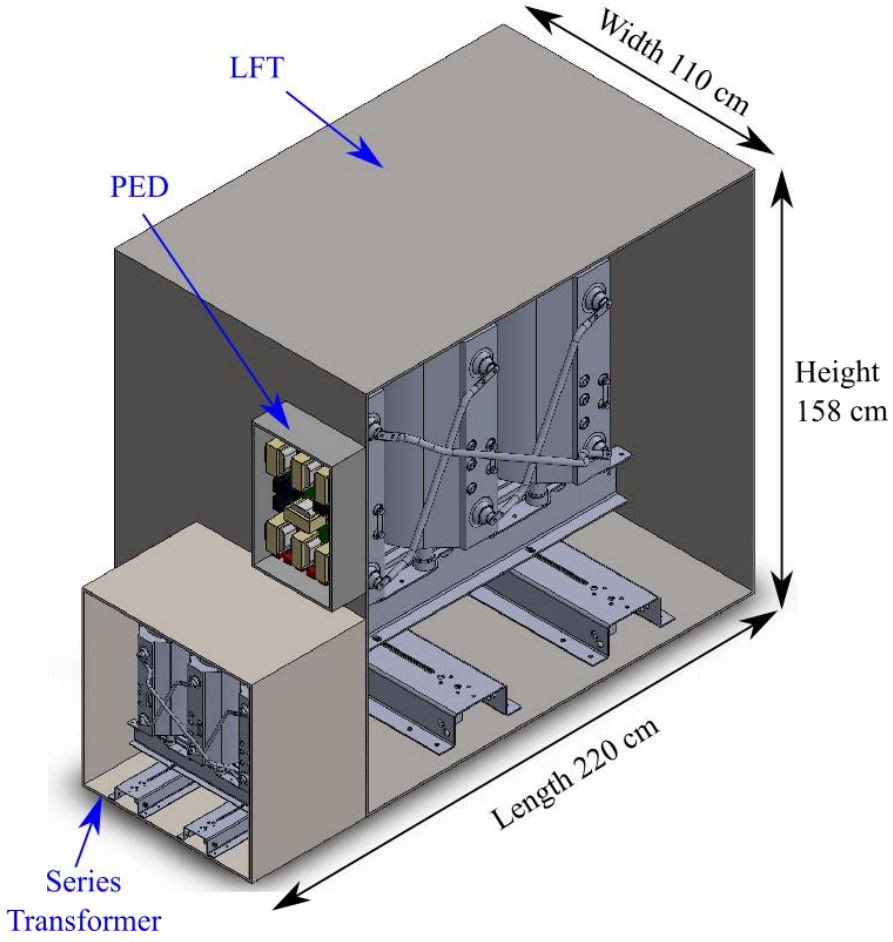
The three-dimensional (3-D) renderings of the D-ST are showcased in Figure 9, reflecting the optimised design outcomes. Figure 9(a) illustrates the configuration where the LFT, PED, and series transformer are all housed within a single cabinet. Conversely, Figure 9(b) displays the arrangement where the LFT, PED, and series transformers are accommodated in separate cabinets. These renderings provide visual representations of the various assembly options, aiding in the evaluation and comparison of design choices for the D-ST.

Based on the 3-D rendering, the estimated dimension of the designed D-ST is 2.20m(Length) × 1.10m(Width) × 1.58m(Height). The 3-D rendering models of the LFT, the PED and the series transformer are presented in Figure 10, Figure 11 and Figure 12, respectively. The 3D-rendering model of the LFT is obtained from Schneider Electric for their 500 kVA 11kV/400V transformer TRI050012579843N00[3]. The 3D-rendering model of the PED is built based on the optimised design results in the previous work packages. The 3-D rendering model of the series transformer is the scaled-down model of the LFT.



(a)

[3] https://www.se.com/au/en/product/TRI050012579843N00/trihal-cast-resin-dry-type-transformer-500-kva-11-kv-43n00/



(b)

Figure 9 3-D rendering of the 500 kVA D-ST including the LFT, PED and series transformer.

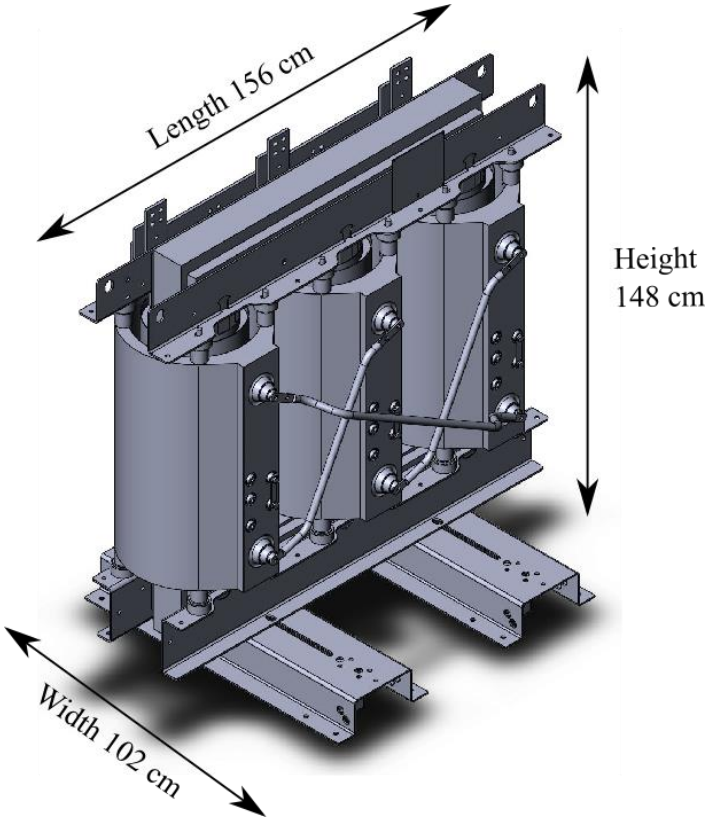


Figure 10 3-D rendering of the 500 kVA 11kV/400V LFT obtained from schneider electric for their product TRI050012579843N00.

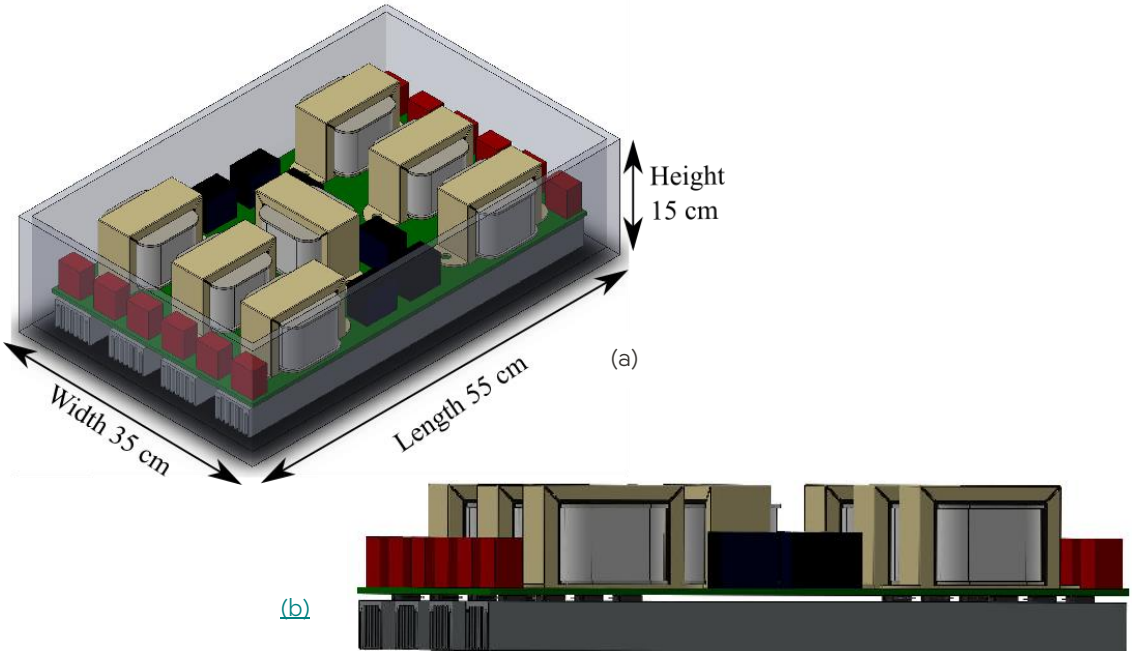


Figure 11 3-D rendering of the 50 kW PED. (a) Isometric view, (b) side elevation.

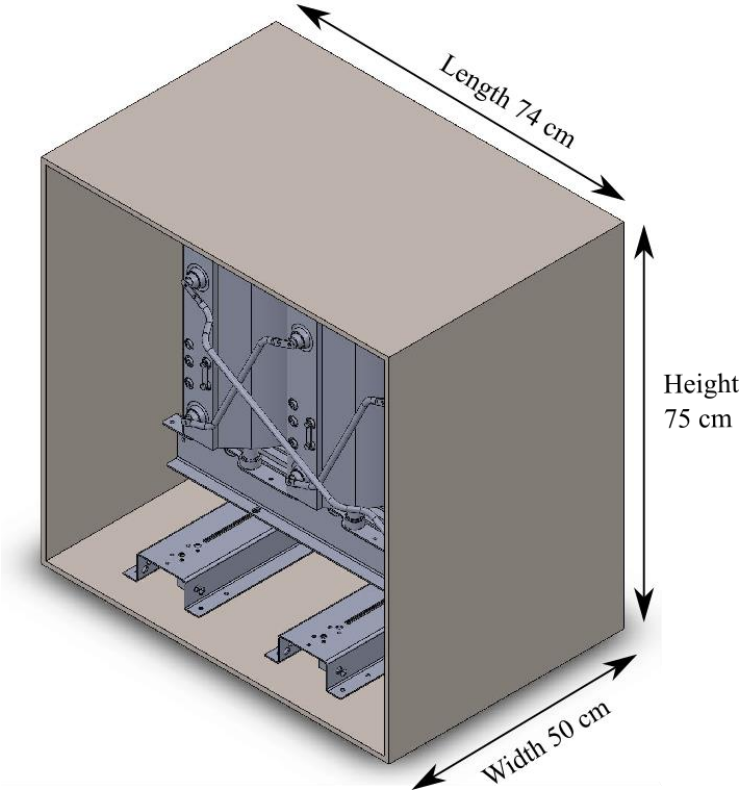


Figure 12 3-D rendering of the 50 kVA 400V/40V series transformer.

7. Conclusions

This report primarily focuses on developing practical requirements for the D-ST, particularly emphasising protection design and dimension estimation. Protection requirements for the D-ST are comprehensively examined across various fault scenarios. External grid faults need the protection of the PED within the D-ST to prevent damage, while internal faults within the PED require a fail-safe operation to ensure uninterrupted functionality of the LFT.

To address these protection needs, a suite of protection mechanisms is designed to protect the PED during critical external grid fault occurrences. Bypass thyristors are implemented to shield the PED from short-circuit faults, while a pre-charging circuit is engineered to mitigate converter inrush current. Furthermore, varistors and a DC-link clamping circuit are integrated to protect the PED from lightning and switching surges, respectively.

Additionally, the report showcases 3D renderings of the D-ST. According to these renderings, the estimated dimension of the D-ST is 2.20m (Length) × 1.10m (Width) × 1.58m (Height). These dimensions align with the project's design requirements and underscore the feasibility and practicality of the presented D-ST solution.

8. Contact Details

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