G83/2 Appendix 4 Type Verification Test Report

Type Approval and manufacturer/supplier declaration of compliance with the requirements of Engineering Recommendation G83/2.			
SSEG Type reference number			
SSEG Type			
System Supplier name			
Address			
Tel		Fax	
E:mail		Web site	

Maximum rated capacity, use separate sheet if more than one connection option.	Connection Option	
		kW single phase, single, split or three phase system
		kW three phase
		kW two phases in three phase system
		kW two phases split phase system

SSEG manufacturer/supplier declaration.
I certify on behalf of the company named above as a manufacturer/supplier of Small Scale Embedded Generators, that all products manufactured/supplied by the company with the above SSEG Type reference number will be manufactured and tested to ensure that they perform as stated in this Type Verification Test Report, prior to shipment to site and that no site modifications are required to ensure that the product meets all the requirements of G83/2.

Signed		On behalf of	

Note that testing can be done by the manufacturer of an individual component, by an external test house, or by the supplier of the complete system, or any combination of them as appropriate.
Where parts of the testing are carried out by persons or organisations other than the supplier then the supplier shall keep copies of all test records and results supplied to them to verify that the testing has been carried out by people with sufficient technical competency to carry out the tests.

Power Quality. Harmonics. The requirement is specified in section 5.4.1, test procedure in Annex A or B 1.4.1						
SSEG rating per phase (rpp)				kW	NV=MV*3.68/rpp	
Harmonic	At 45-55% of rated output		100% of rated output			
	Measured Value (MV) in Amps	Normalised Value (NV) in Amps	Measured Value (MV) in Amps	Normalised Value (NV) in Amps	Limit in BS EN 61000-3-2 in Amps	Higher limit for odd harmonics 21 and above
2					1.080	
3					2.300	
4					0.430	
5					1.140	
6					0.300	
7					0.770	
8					0.230	
9					0.400	
10					0.184	
11					0.330	
12					0.153	
13					0.210	
14					0.131	
15					0.150	
16					0.115	
17					0.132	
18					0.102	
19					0.118	
20					0.092	
21					0.107	0.160

22					0.084	
23					0.098	0.147
24					0.077	
25					0.090	0.135
26					0.071	
27					0.083	0.124
28					0.066	
29					0.078	0.117
30					0.061	
31					0.073	0.109
32					0.058	
33					0.068	0.102
34					0.054	
35					0.064	0.096
36					0.051	
37					0.061	0.091
38					0.048	
39					0.058	0.087
40					0.046	
Note the higher limits for odd harmonics 21 and above are only allowable under certain conditions, if these higher limits are utilised please state the exemption used as detailed in part 6.2.3.4 of BS EN 61000-3-2 in the box below.						

Power Quality. Voltage fluctuations and Flicker. The requirement is specified in section 5.4.2, test procedure in Annex A or B 1.4.3								
	Starting			Stopping			Running	
	d_{max}	d_c	$d_{(t)}$	d_{max}	d_c	$d_{(t)}$	P_{st}	P_{lt} 2 hours
Measured Values								
Normalised to standard impedance and 3.68kW for multiple units								
Limits set under BS EN 61000-3-2	4%	3.3%	3.3% 500ms	4%	3.3%	3.3% 500ms	1.0	0.65

Test start date		Test end date		
Test location				

Power quality. DC injection. The requirement is specified in section 5.5, test procedure in Annex A or B 1.4.4				
Test power level	10%	55%	100%	
Recorded value				
as % of rated AC current				
Limit	0.25%	0.25%	0.25%	

Power Quality. Power factor. The requirement is specified in section 5.6, test procedure in Annex A or B 1.4.2				
	216.2V	230V	253V	Measured at three voltage levels and at full output. Voltage to be maintained within ±1.5% of the stated level during the test.
Measured value				
Limit	>0.95	>0.95	>0.95	

Protection. Frequency tests The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.3						
Function	Setting		Trip test		"No trip tests"	
	Frequency	Time delay	Frequency	Time delay	Frequency /time	Confirm no trip
U/F stage 1	47.5Hz	20s			47.7Hz 25s	
U/F stage 2	47Hz	0.5s			47.2Hz 19.98s	
					46.8Hz 0.48s	
O/F stage 1	51.5Hz	90s			51.3Hz 95s	
O/F stage 2	52Hz	0.5s			51.8Hz 89.98s	
					52.2Hz 0.48s	

Protection. Voltage tests The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.2						
Function	Setting		Trip test		"No trip tests"	
	Voltage	Time delay	Voltage	Time delay	Voltage /time	Confirm no trip
U/V stage 1	200.1V	2.5s			204.1V 3.5s	
U/V stage 2	184V	0.5s			188V 2.48s	
					180V 0.48s	
O/V stage 1	262.2V	1.0s			258.2V 2.0s	
O/V stage 2	273.7V	0.5s			269.7V 0.98s	
					277.7V 0.48s	
Note for Voltage tests the Voltage required to trip is the setting ±3.45V. The time delay can be measured at a larger deviation than the minimum required to operate the protection. The No trip tests need to be carried out at the setting ±4V and for the relevant times as shown in the table above to ensure that the protection will not trip in error.						

Protection. Loss of Mains test. The requirement is specified in section 5.3.2, test procedure in Annex A or B 1.3.4						
To be carried out at three output power levels with a tolerance of plus or minus 5% in Test Power levels.						
Test Power	10%	55%	100%	10%	55%	100%
Balancing load on islanded network	95% of SSEG output	95% of SSEG output	95% of SSEG output	105% of SSEG output	105% of SSEG output	105% of SSEG output
Trip time. Limit is 0.5 seconds						
For Multi phase **SSEG**s confirm that the device shuts down correctly after the removal of a single fuse as well as operation of all phases.						
Test Power	10%	55%	100%	10%	55%	100%
Balancing load on islanded network	95% of SSEG output	95% of SSEG output	95% of SSEG output	105% of SSEG output	105% of SSEG output	105% of SSEG output
Trip time. Ph1 fuse removed						
Test Power	10%	55%	100%	10%	55%	100%
Balancing load on islanded network	95% of SSEG output	95% of SSEG output	95% of SSEG output	105% of SSEG output	105% of SSEG output	105% of SSEG output
Trip time. Ph2 fuse removed						
Test Power	10%	55%	100%	10%	55%	100%
Balancing load on islanded network	95% of SSEG output	95% of SSEG output	95% of SSEG output	105% of SSEG output	105% of SSEG output	105% of SSEG output
Trip time. Ph3 fuse removed						
Note for technologies which have a substantial shut down time this can be added to the 0.5 seconds in establishing that the trip occurred in less than 0.5s. Maximum shut down time could therefore be up to 1.0 seconds for these technologies.						
Indicate additional shut down time included in above results.					ms	
Note as an alternative, inverters can be tested to BS EN 62116. The following sub set of tests should be recorded in the following table.						
Test Power and imbalance	33% -5% Q Test 22	66% -5% Q Test 12	100% -5% P Test 5	33% +5% Q Test 31	66% +5% Q Test 21	100% +5% P Test 10
Trip time. Limit is 0.5s						

Protection. Frequency change, Stability test The requirement is specified in section 5.3.3, test procedure in Annex A or B 1.3.6				
	Start Frequency	Change	End Frequency	Confirm no trip
Positive Vector Shift	49.5Hz	+9 degrees		
Negative Vector Shift	50.5Hz	- 9 degrees		
Positive Frequency drift	49.5Hz	+0.19Hz/sec	51.5Hz	
Negative Frequency drift	50.5Hz	-0.19Hz/sec	47.5Hz	

Protection. Re-connection timer. The requirement is specified in section 5.3.4, test procedure in Annex A or B 1.3.5						
Test should prove that the reconnection sequence starts after a minimum delay of 20 seconds for restoration of voltage and frequency to within the stage 1 settings of table 1.						
Time delay setting	Measured delay		Checks on no reconnection when voltage or frequency is brought to just outside stage 1 limits of table 1.			
			At 266.2V	At 196.1V	At 47.4Hz	At 51.6Hz
Confirmation that the SSEG does not re-connect.						

Fault level contribution. The requirement is specified in section 5.7, test procedure in Annex A or B 1.4.6					
For a directly coupled SSEG			For a Inverter SSEG		
Parameter	Symbol	Value	Time after fault	Volts	Amps
Peak Short Circuit current	i_p		20ms		
Initial Value of aperiodic current	A		100ms		
Initial symmetrical short-circuit current*	I_k		250ms		
Decaying (aperiodic) component of short circuit current*	i_{DC}		500ms		
Reactance/Resistance Ratio of source*	X/R		Time to trip		In seconds

Self-Monitoring solid state switching The requirement is specified in section 5.3.1, No specified test requirements.	Yes/or NA
It has been verified that in the event of the solid state switching device failing to disconnect the SSEG, the voltage on the output side of the switching device is reduced to a value below 50 volts within 0.5 seconds.	

Additional comments