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SP ENERGY NETWORKS

LV ENGINE

Solid State Transformer - Detailed Design

About Report		
Report Title	:	LV Engine #2 - Solid State Transformer – Detailed design
Report Status	:	Final
Project Reference	:	LV Engine

Contents

Glossary of Terms

Abbreviation	Definition
DAB	Dual Active Bridge
EGB	ERMCO-Gridbridge
HV	High Voltage (11kV)
LV DC	Low Voltage Direct Current
NIC	Network Innovation Competition
SCS	Smart Control System
SiC	Silicon Carbide (High speed, low loss switching semiconductor)
SPEN	SP Energy Networks
SSR	Solid State Relay
SST	Solid State Transformer
TAB	Triple Active Bridge
TRL	Technology Readiness Level
UPFC	Unified Power Flow Controller

Disclaimer

This report has been prepared as part of the LV Engine project, a globally innovative project to demonstrate the functionalities of a Smart Transformer, funded by Ofgem through the Network Innovation Competition mechanism. All learnings, outcomes, models, findings information, methodologies or processes described in this report have been presented based on the information available to the project team at the time of publishing. In particular, it should be noted the material reported at this stage are subject to modifications as a result of new findings from the product design process, prototyping and benchtop testing exercises. It is at the discernment and risk of the reader to rely upon any learnings outcomes, findings, information, methodologies or processes described in this report.

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Executive Summary

Aim of this report

This report provides the detailed design of power electronic devices which will be designed, manufactured and trialled in LV Engine project. The design information presented in this report is based on materials developed and information available at the time of writing this report. The report is one of the two reports which have been prepared to satisfy Deliverable 2 specified in LV Engine Project Direction.

Reference	Project Deliverable	Evidence
Deliverable 2	Detailed technical design of SST by the manufacturer and life cycle assessment.	Production of two documents: 1. Detailed design: The information will be provided as much as it complies with IRP agreement with the manufacturing partner, that can include the topology (stages) of SST, the cooling system, the choice of conductor, the control algorithm, SST protection logic, and all the lessons learnt within WP 3. 2. Life cycle assessment: The results of life cycle assessment based on manufacturing and material process which will be conducted by an academic or consultant partner.

The report structure is as follows:

- Executive summary – Providing high level aspects of the SST design for both topologies and key lessons learnt;
- Section 1, 2 and 3 – Introduction to LV Engine, core functionalities and the power electronic products which will be developed in LV Engine;
- Section 4 – Detailed design of SST Topology 1 – Power electronic device added to the conventional transformer;
- Section 5 – Detailed design of SST Topology 2 and challenges identified – Full power electronic transformer;
- Section 6 – Lessons Learnt and Next step;
- Appendices – The detailed design of back to back (AC/DC/AC) as a potential design for SST Topology 1 is provided in Appendix A but it should be noted this design will not be implemented in LV Engine as a more efficient design described in Section 4 was developed. The results of extensive simulations carried out to demonstrate the operation of the SST in radial and interconnected LV networks are also presented in Appendix B.

LV Engine overview

LV Engine is one of SP Energy Networks (SPEN) flagship projects funded through Network Innovation Competition (NIC) mechanism. This project aims to design and trial Smart Transformers (ST) within the distribution network at secondary substations (11kV/0.4kV) to enhance network flexibility and release

additional capacity within the existing low voltage (LV) infrastructure[1]. If successful, the LV Engine solution can significantly facilitate the uptake of low carbon technologies (e.g. Photovoltaics, Electric Vehicles).

A ST consists of a Solid-State Transformer (SST) and a Smart Control System (SCS). SST uses power electronic technologies to deliver several functionalities, SCS, however, provides the control set points to SST based on data gathered and analysed from different monitored points in the network. LV Engine aims to demonstrate the following Core Functionalities can be delivered by deploying SST at secondary substations:

- Voltage regulation at LV Networks;
- Capacity sharing with other substations;
- Cancelation of LV imbalance load seen by the HV network;
- Reactive power compensation and power factor correction at secondary substations;
- Provision of LV DC to supply rapid and ultra-rapid EV chargers.

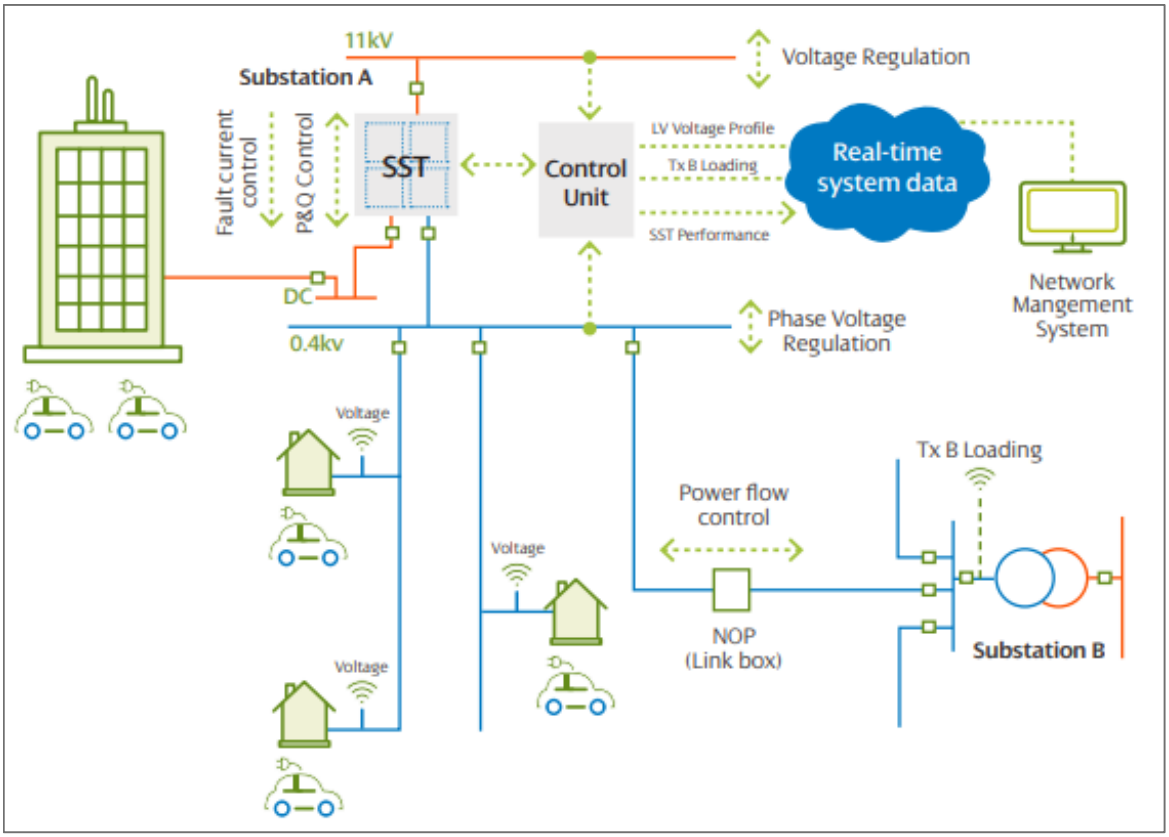


Figure 1 – LV Engine project concept

LV Engine power electronics products

As the focus of the LV Engine project is demonstrating the performance of the Core Functionalities required by the network, any SST innovative topology that provide these Core Functionalities in an efficient and reliable manner at secondary substation was considered. There are different possible SST topologies which have been considered as products of LV Engine:

- ***Topology 1*** *- Topology using a conventional low frequency 50Hz (LF) transformer* –This topology uses power electronics devices at the secondary side of conventional LF transformers (11kV/0.4kV). The power electronic devices can be added to the existing distribution

[1] https://www.spenergynetworks.co.uk/pages/lv_engine.aspx

transformers to deliver the Core Functionalities of LV Engine. The aim is to enhance Technology Readiness Level (TRL) of this product from 6 to 9.

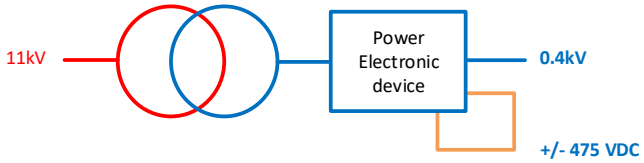


Figure 2 SST Topology 1

- ***Topology 2*** - *Topology using a High Frequency (HF) transformers* – Using HF Transformers and power electronics may allow a modular and compact design while delivering the LV Engine Core Functionalities. SPEN recognises that this topology may require a larger effort for design and manufacturing compared to the approach of retrofitting an LF transformer with power electronics. The aim is to enhance TRL of this product from 5 to 8.

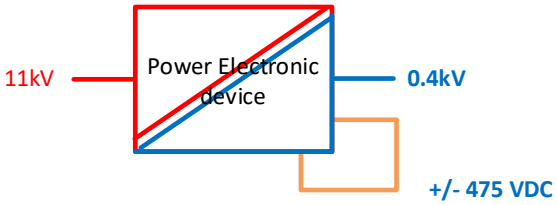


Figure 3 SST Topology 2

Summary of the design

Following a competitive tender conducted in 2019, ERMCO-Gridbridge (EGB) was appointed as LV Engine SST manufacturing partner in November 2019. After staff mobilisation, EGB commenced the design process for both SST Topologies in early Q1 2020. The design process was initiated through the Project Inception phase, where regular detailed discussions with the SPEN team were held to translate each of the technical/functional requirements specified within the Smart Transformer Technical Specifications[1] (LV Engine's Deliverable #1) to an element of the electrical, control and mechanical design. As part of project inception phase, EGB/SPEN team attended familiarisation sessions to review typical LV/HV operation practices in the UK and visit typical SPEN's secondary substations. A summary of product development process for the two SST topologies is shown in Figure 5. It is planned that the Prototyping phase starts in December 2020.

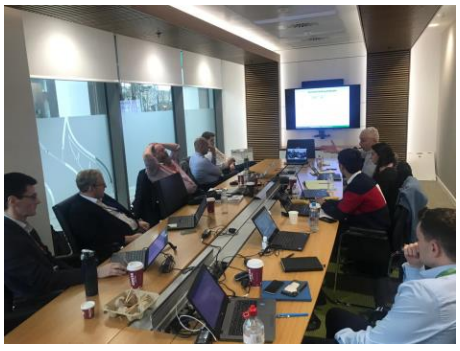


Figure 4 - Network operation familiarisation and site visits took place with EGB team in February 2020

1 https://www.spenergynetworks.co.uk/userfiles/file/LV_Engine_Deliverable1_Smart_Transformer_Technical_Specification_REDACTED.pdf

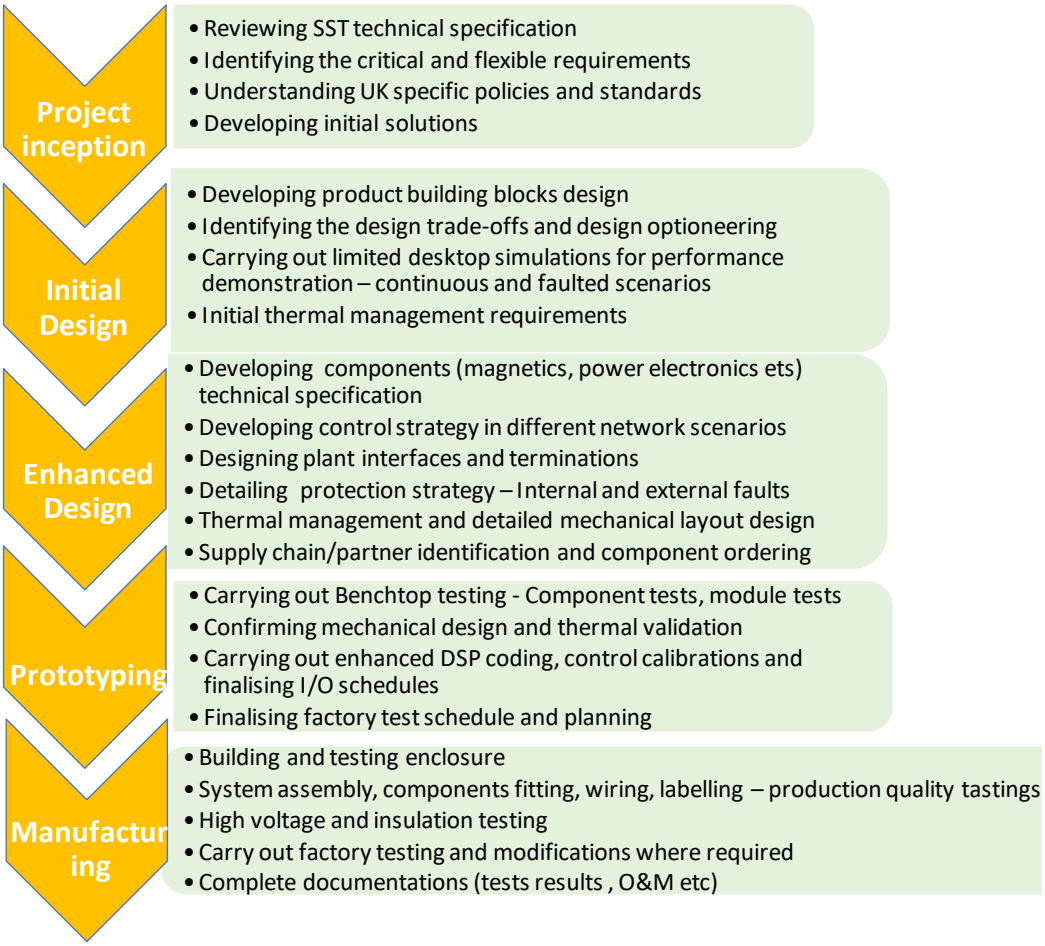


Figure 5 – SST development process

SST Topology 1

Building block design

The high-level system architecture initially considered for SST Topology 1 is shown in Figure 6. The components inside of the grey box indicate the components that EGB are responsible to deliver. The dotted lines indicate isolation barriers.

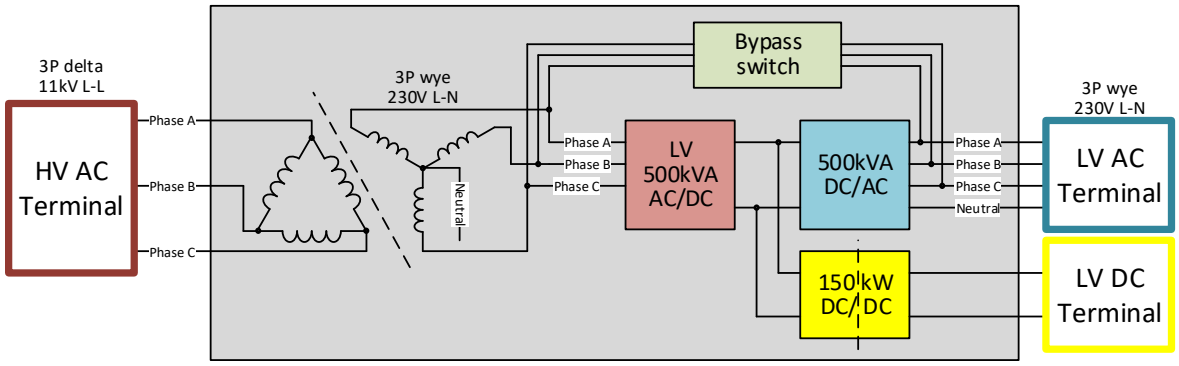


Figure 6 SST Topology 1 Block Diagram – Initial design considered

Nonetheless, following the detailed design analysis, performance evaluation and mechanical design of SST Topology 1, it was decided to consider Unified Power Flow Controller (UPFC) architecture for SST Topology 1 as shown in Figure 7. This decision was based on various product

analysis carried out by EGB and SPEN team with the aim to improve the reliability and adaptability of the product for business as usual deployment. The main advantages of the UPFC (Figure 7) over the back to back conversion architecture (Figure 6) are as follows:

- **Improved performance during the fault –** Providing the same level of fault contribution to the faulted LV network as conventional transformer, eliminating the issue of low fault current provision by power electronics;
- **Improved efficiency –** The efficiency is expected to achieve 99% with the UPFC design as the power electronics do not need to supply all the LV demand and only operates to provide the system services. This will improve the efficiency and life-time losses significantly as the initial back to back design efficiency target was expected to be around 97%;
- **Smaller power electronics power rating –** For the same reason explained above, nominal power capability of the power electronics can be reduced significantly. This reduces the design complication and the overall system cost;
- **Bypass possibility –** The UPFC design is fail-safe bypassing the power electronic unit when it is not needed or if there is any issue with power electronic components;
- **Smaller dimensions –** The lower power electronics power rating, higher efficiency and capability to bypass during the fault conditions contribute to a more compact physical layout design compared to the back to back design;
- **Better reliabilities and building on previous EGB experience –** SST Topology 1 will be the first product of its type with no previous experience in the field, so the reliability of the product is yet to be seen in a live trial although reliability is evident in the design. EGB has existing 3 phase 150kW UPFC product which is currently commercially ready, however this product does not deliver all the functionalities required in LV Engine and is not designed to UK standards.

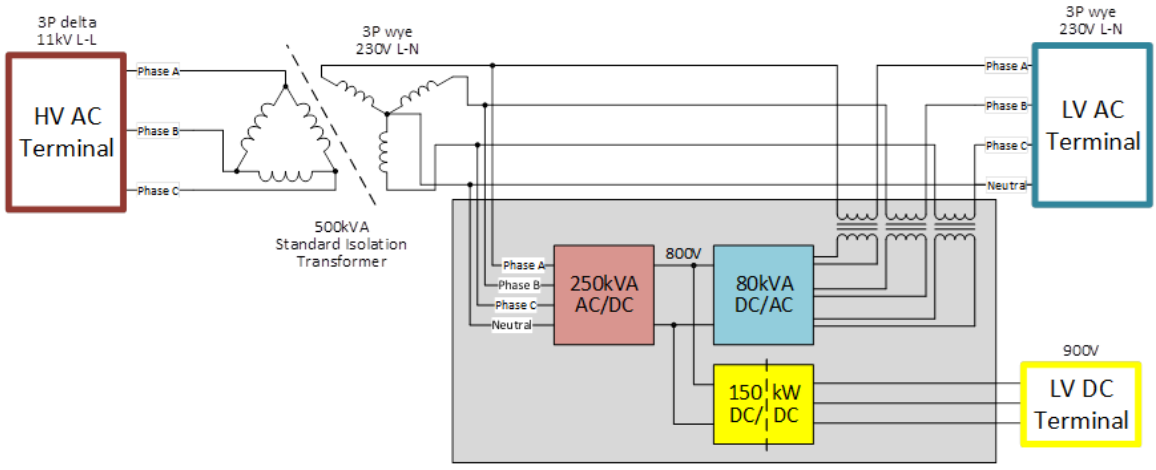


Figure 7 SST Topology 1, UPFC architecture

Technical specification

The nominal system specifications for the LV Engine SST Topology 1 are outlined in Table 1.

Table 1 LV Engine ST Topology 1 nominal system specifications

Operating conditions	Specification	Notes
Nominal power rating	500kVA	Maximum rating
Nominal load current	725Arms	500kVA@230Vrms
Nominal system frequency	50 Hz	-
Delta/Wye configuration	Wye in, Wye out	-
Operational modes	Radial or Mesh	V or I control
Nominal input voltage	249Vrms L-N	433Vrms L-L
Nominal output voltage	230Vrms L-N	400Vrms L-L
Operating temperature range	-25C to +40C	Worst case limits
Imbalance control	30%	Max correction
Power Factor Control (PFC)	0.893 to 1.0 PF	Max per phase
Output voltage control range	38.6Vrms L-N	+ or – to input
DC Service @ +/- 475VDC	150kW Total	75kW per polarity

Control strategy

In order to deliver the LV Engine Core Functionalities, SST may operate in a radial or interconnected LV network arrangement. In an interconnected LV network, SST should be able to control the power flow within the interconnection following the control power command received from Smart Control System (SCS). An SST power flow control strategy has been developed to deliver the Core Functionalities while ensuring voltage stability and quality of supply to electricity customer stays within statutory limits. Extensive desktop studies presented in 6.2Appendix AAppendix B were carried out to demonstrate the performance in radial and interconnected network arrangements.

Mechanical layout and local interface

The SST Topology 1 mechanical packaging will be confined to a (1.0m x 1.0m x 1.5m) overall envelope size (with ±10% variation) including all required cooling apparatus and cable boxes. This has been the target design and is being finalised with the aim to include the factory ordered optional 150kW DC Service Module in the target envelope size. The latest layout design is shown in Figure 8.

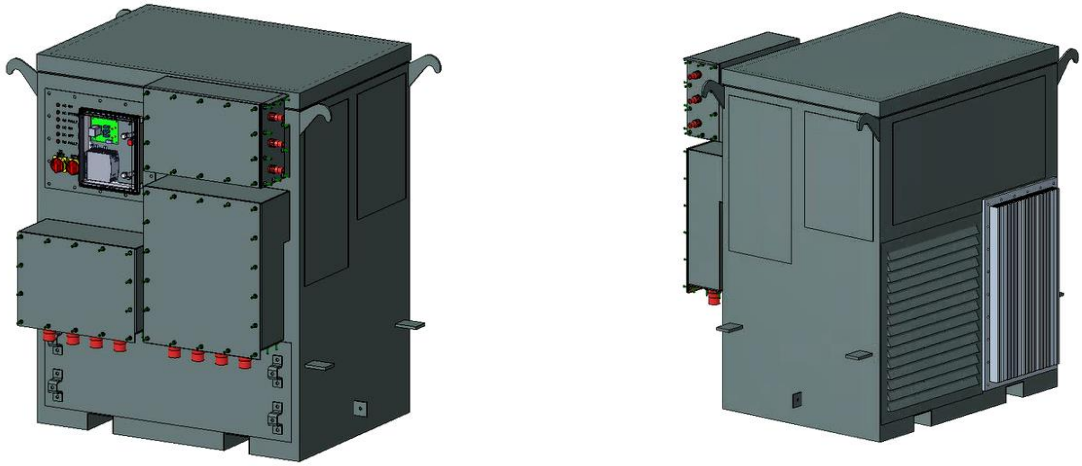


Figure 8 Physical layout of the SST Topology 1

The local interface design, shown in Figure 9, provides operation staff with the flexibility to switch off the power electronic and operate the unit in bypass mode. The following functions will be provided by the local interface:

- Providing indicators confirming the operation status;
- Access to switches providing the option for the local operation staff to switch off/on the power electronics that includes bypassing the AC services and coupling transformer, and switching off the DC operation;
- Connection to the Ethernet port for communication with SPEN telecoms/router with which communicating control commands, monitored parameters and remote access is facilitated;
- Access to auxiliary power supply providing 24DC for HV switchgear inter-tripping scheme and supply for the telecoms with secondary substation;
- Access to the contactor relay for connection of the 24VDC to HV switchgear's shunt trip coil;
- Provide a test point (via a multi-meter device) for the operation staff to ensure no internal capacitor charge exists before any work on the device.

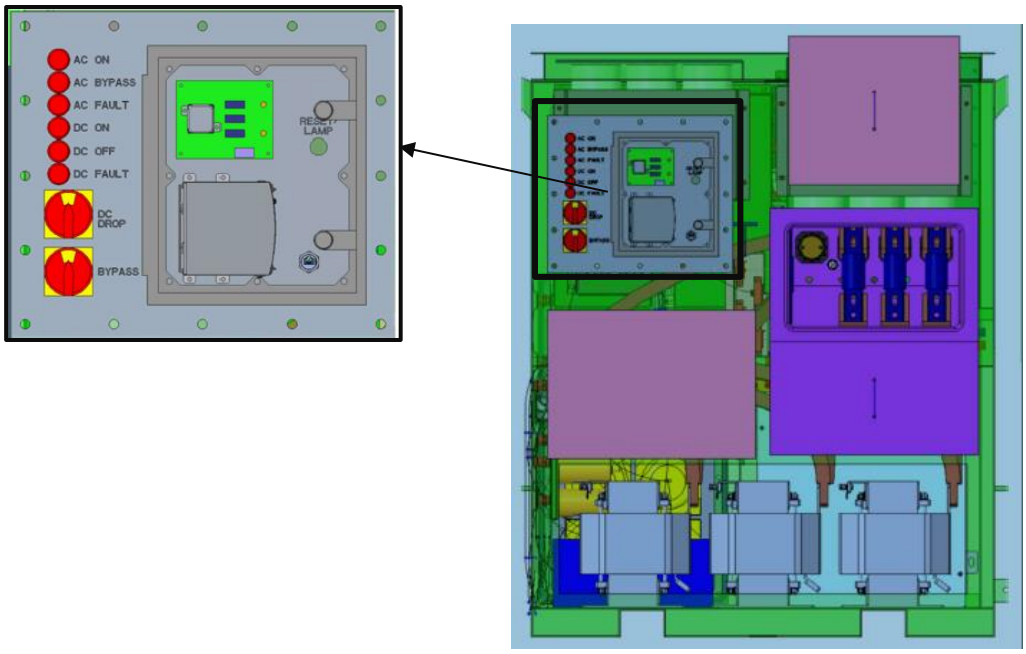


Figure 9 SST Topology 1, Local interface

Next step

The materials and component of the SST Topology 1 have now been completely ordered and they are expected to be delivered within late Q4 2020 and early Q1 2021. According to the design and manufacturing plan, prototyping and benchtop testing are the main activities and will start in Q1 2021. Manufacturing and Factory testing will commence in Q2 2021 with design changes and product manufacturing and testing completed in Q3 2021.

SST Topology 2

SST Topology 2 is a more complicated product development endeavour compared to SST Topology 1. As a result of that, the design progress is not as advanced as Topology 1 at the time of writing this report. Nonetheless, significant work has been carried out to detail the challenges, establish the topology and identify the requirements for operation under different network conditions. The detail design aspects developed to date have been documented in this report. EGB team have been

successfully engaging with academic and industrial partners to adopt the solutions which have already been developed so that the design process for LV Engine product can be optimised.

Building block design

The overall building block of SST Topology 2 is shown in Figure 10. SST Topology 2 consist of three stages: the HV AC/DC stage, isolated DC/DC stage and DC/AC stage.

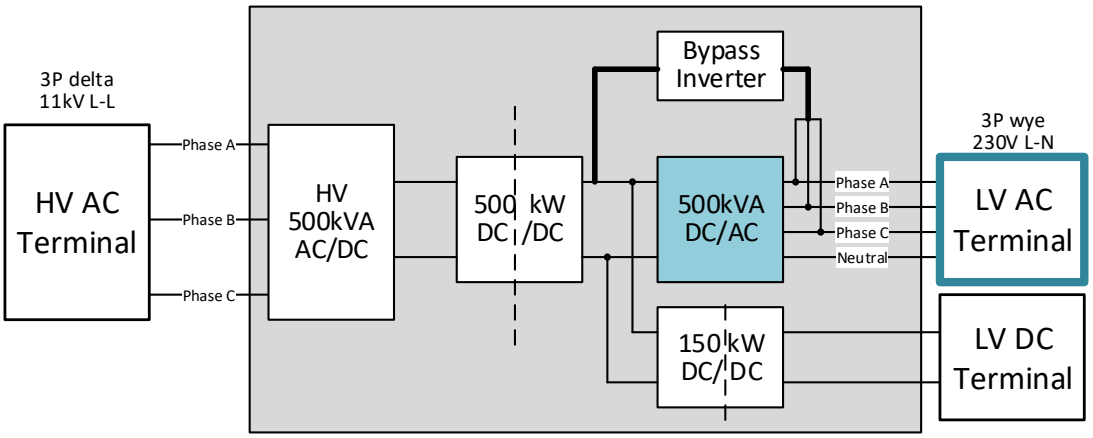


Figure 10 HV-SST 500kVA DC/AC Inverter feeds the LV-AC Terminal

There are several challenges in developing the SST Topology 2 rectifier stage and isolated DC/DC stage. There are ongoing works by EGB on strengthening university research relationships having a background in SST research to further better simulate and investigate the topology and hardware options for the SST input power stages. As part of this, several options have been explored to narrow the focus, highlight any challenges, and underscore requirements above, current research study and previous experiences of EGB team. The focus is currently on the following challenges[1]:

1. Due to the vulnerability to overvoltage of the power semiconductor devices, proper protection methods should be taken to meet the isolation requirements. As specified by IEC 60076-3, SST Topology 1 should comply with the 75kV lightning impulse and 28kV withstand voltage;
2. The design of SST should leave sufficient margin for operational overvoltage up to 19.4kV peak;
3. Due to the limited overcurrent capacity of the power semiconductor devices, to handle the LV short circuit fault adequately to blow the downstream fuses, the power output of the HV stage should be oversized by 100% to about 1.0MVA for 3 seconds;
4. The utilisation of multi-level structure shown in Figure 11 due to the availability of HV commercial semiconductor devices increases the number of components and control complexity. In total there are 378 additional critical components required for the HV-LV conversion alone. This does not include the additional DSPs and Control Processors required to drive the 42 Si IGBTs and 84 SiC MOSFETs required.

The high voltage to low voltage conversion is accomplished via the 500kVA AC/DC high voltage rectifier and isolated DC/DC converter. The purpose of the HV 500kVA AC/DC rectifier is to take the three-phase high-voltage input and transform it to a cascaded medium voltage dc bus. The 500kW DC/DC then interfaces with the high voltage rectifier to provide isolation and control for the internal low voltage dc bus.

[1] In Nov 2020, EGB team informed SPEN that after extensive engagement with academic and industrial partners, they have concluded that they would use a new 2.0kV SiC modules from a Tier 1 power semiconductor supplier which will be commercially sampled for prototyping in Q1 2021. Using these modules will significantly reduce the number of components contributing to considerable improvement in size, reliability and overall cost of the unit.

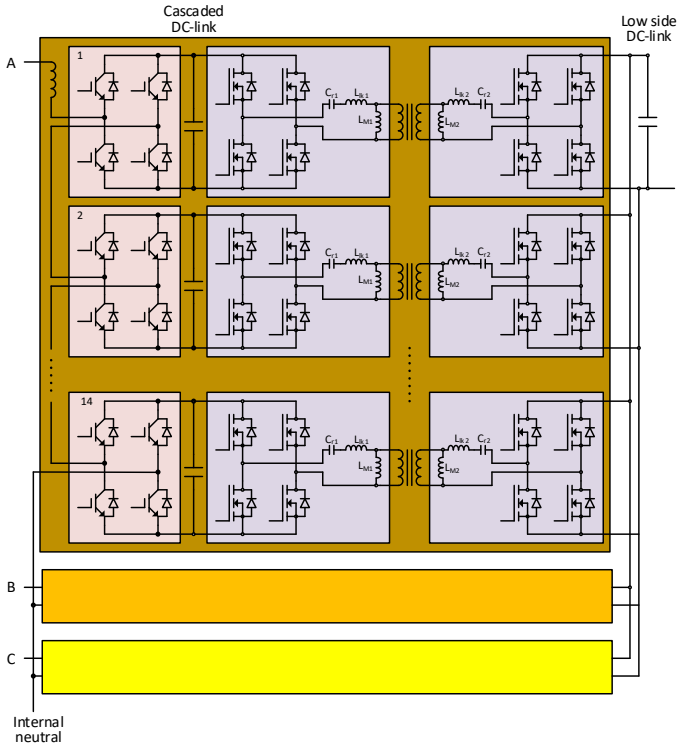


Figure 11 Input Rectifier and DC/DC Stage Possible Topology – 42 Stages Required

Academic and Industry engagement

To accelerate progress and break ground on the challenges, specifically the HV to Isolated DC conversion, EGB agreed to add additional qualified resources and/or key technology to the SPEN SST Topology 2 development program. EGB pursued noted power electronics programs at four universities where existing relationships exist:

1. University of Texas, Austin: Semiconductor Power Electronics Center (SPEC) – Dr. Alex Q. Huang (SPEC Director)
2. North Carolina State University: NSF FREEDM Systems Center – Dr. Iqbal Hussain (FREEDM Director)
3. Virginia Tech: Future Energy Electronics Center (FEEC) – Dr. Jason Lai (FEEC Director)
4. University of Colorado, Boulder: Colorado Power Electronics Center (CoPEC) – Dr. Dragan Maksimovic

EGB evaluated the technology developments at SPEC (UT-A), FREEDM (NCSU) and FEEC (VT) for possible commercial advancement for use in the LV Engine application. After evaluation and additional research, the detailed technology advancement focused on UT-A that revealed an unfolding Bridge & DAB topology using an experimental "SuperMOS" Cascade 7.2kV SiC module and experimental HV DAB Transformer[1]. This solution is currently an early single-phase lab prototype and after series of deep technical evaluation, risks/rewards assessment and due diligence EGB concluded that the UT-A prototype cannot be deployed in LV Engine development.

EGB has also re-engaged Mitsubishi, Infineon & Wolfspeed for an update on their commercially available Si and SiC switching devices based on lessons learnt relating to topology, partitioning, modularity, reducing risk, best industry practice & commercial availability of the required supporting circuits (gate drive, power supplies, sensors). The main output of these engagements was to learn that 2.0kV SiC devices will be commercially available in Q2 2021 by Infineon with early access in Q1 2021.

[1] https://repository.lib.ncsu.edu/bitstream/handle/1840.20/34943/etd.pdf?sequence=1&isAllowed=y

This can significantly reduce overall SST Topology 2 cost, improve reliability, reduce cooling requirements and size of the product developed for LV Engine.

Next Steps

EGB is currently validating the power and thermal simulation of the Infineon 2.0kV SiC modules. In anticipation of successful power & thermal simulation results with the 2.0kV SiC modules, EGB has agreed with Infineon to reserve parts for early benchtop prototype work in Q1 2021, ordering materials in Q2, the prototyping and manufacturing are scheduled in Q3 2021.

Key Lessons Learnt

The detailed design of SST topologies and components considered are provided in this report. Although each section of this report provides specific learning about the LV Engine products, a summary of key learnings is listed below:

- The UPFC design is preferable over the back to back (AC/DC/AC) design for SST Topology 1 solution. As the UPFC design offers a more efficient, smaller footprint, more reliable and less expensive solution than the back to back design. In addition, UPFC does not limit the fault current to the LV network whereas back to back arrangement does have this limitation;

- The status of LV network (radial or interconnected) may not be available to SST in a real-time basis, therefore the control strategy for delivery of SST services (e.g. voltage control or power flow control) should not rely on the real-time information from network;

- The voltage at SST LV terminal should remain stable in the event of sudden change in demand to ensure the quality of supply to the customers is not affected. For that reason, SST control strategy in response to active (P) and reactive power (Q) setpoints is to revert to voltage control mode after achieving the setpoint. In another words, SST will not lock to the P&Q set points after achieving them but will lock to the resultant voltage after achieving P&Q set points;

- The services expected from SST (e.g. voltage control, imbalance cancelation, power factor correction etc) at full rating may not be required at the same time. Designing SST for provision of all services concurrently at full rating leads to unnecessarily overdesigning the product. Instead, priority of services can be considered so that some of the services may gracefully degraded if SST reaches its thermal ratings;

- For devices connected to the HV network, the insulation requirements are to pass the impulse lightening voltage of 75kV and withstand voltage of 28kV in compliance with IEC 60076-3. In SST Topology 2 will have power electronic modules connected directly to the HV network. Although the bushing and insulation to the enclosure can be designed to satisfy IEC 60076-3 power electronic devices are very susceptible to excessive overvoltage condition. Therefore, some specific design considerations should be considered to protect the power electronic modules in overvoltage conditions. LV Engine's existing design is to stack up extra power electronic modules at HV to build the tolerance against 28kV however further design options to meet the 75kV lightening impulse are being assessed;
- The safety policy for working around grid connected capacitor devices should be considered for power electronic devices too. Capacitors may be used in the design of a power electronic device, for example SST requires an internal DC link which is constructed by series of capacitors. In order to avoid any capacitor charge shock to operation staff, SST should be fitted with a discharging mechanism. Also, operation staff should be able to test internal charges using multi-meters and test points available on SST local interface before conducting any work on SST (e.g. replacing the fuses).

- SST design for LV Engine will provide 24V DC supply through the local interface. This can be used for any telecommunication supply with no need for extra auxiliary supply in the substation. SST will also be able to issue 24V DC inter-tripping voltage to the ring main unit (shunt trip coil) which will be used in overall protection strategy.

- The spare parts required for SST should be available in the substation to ensure operation staff can have immediate access to spare parts in case of failure. SST designed in LV Engine has an allocated compartment for the spare parts especially 800A fuses.

- Power electronic devices may have limited capability in temporary overloading and adequate fault current contribution to allow operation of protection devices based on existing operation practices. More innovative solutions for fault identification and protection should be developed if power electronics are to be effectively deployed in both AC and DC distribution networks.

1. Introduction

LV Engine is one of SP Energy Networks flagship projects funded through Network Innovation Competition (NIC) mechanism. This project aims to design and trial Smart Transformers (ST) within the distribution network at secondary substations (11kV/0.4kV) to enhance network flexibility and releasing additional capacity within the existing low voltage (LV) infrastructure. It is envisaged that the ST consists of two main components:

1. **Solid-State Transformer (SST):** This unit includes digitally controlled power electronics and hardware which provide various network control functionalities. The SST will be installed in tSecondary Substations and provide voltage conversion from High Voltage (HV) (11kV) to Low Voltage (0.4kV). SST can control the power flow passing through itself and voltage at its terminals by adjusting the power electronics switching in response to set points received from the Smart Control System (SCS).

2. **Smart Control System (SCS)**: This system includes a number of intelligent units which provide the control set points to SST based on the data monitored at different points in the LV and HV network. SCS has an operational supervisory capability to estimate the latest operation conditions and requirements within a regional control zone to satisfy network optimisation objectives and constraints.

Following a competitive tendering process, ERMCO-GridBridge (EGB) was appointed as the SST Manufacturing Partner. EGB started the product design in January 2020. This report aims to provide the electrical, mechanical and control design elements of Solid State Transformers (SST) which will be manufactured within LV Engine project. It should be noted the materials reported at this stage are subject to modifications as a result of new findings from the product design process, prototyping and benchtop testing exercises.

This report is prepared as part of the second LV Engine deliverable as specified in LV Engine Project Direction[1].

2. LV Engine core functionalities

LV Engine aims to enhance LV networks operation by adding intelligent controls and automation functionalities to Secondary Substations. A general concept of the LV Engine is shown in Figure 12. LV Engine will trial STs in a number of schemes to demonstrate various Core Functionalities including:

- *Phase Voltage Regulation* – The overall voltage profile of an LV feeder can be optimised by intelligently adjusting the phase voltage in real-time at the Secondary Substation in response to monitored voltage data points along the length of each LV feeder.
- *Power Flow Control* – STs have the capability to control power flow due to the inclusion of power electronics. This allows an ST to load share with nearby conventional transformers in real time for the purposes of reducing the thermal strain at peak times and maximising network capacity.
- *Reactive Power Control* – An ST can offer independent voltage regulation at the LV and HV terminals. Reactive power support and local voltage regulation at the HV terminal can be deployed to improve the voltage profile along the HV network. This function can be complementary to the conventional Automatic Voltage Control (AVC) scheme at the upstream Primary Substations.
- *Low Voltage Direct Current (DC) Supply* – Conversion of voltage from HV to LV by use of power electronics provides access to a DC voltage at the Secondary Substation. A DC connection can be made available to satisfy any local DC demand, renewable energy sources (RES), or energy

[1] https://www.ofgem.gov.uk/system/files/docs/2018/01/lve_-_project_direction.pdf

storage without repeated rectification from AC to DC and the resulting network and customer losses. Running the LV network at DC can also increase the transfer capacity of the network allowing more Electric Vehicle (EV) load to connect to the network before costly network reinforcement is required.

- *Imbalance Load cancelation* – The LV imbalance load transferred to the HV network can be cancelled by the ST so the HV network only sees balanced load supplied by the secondary substation.

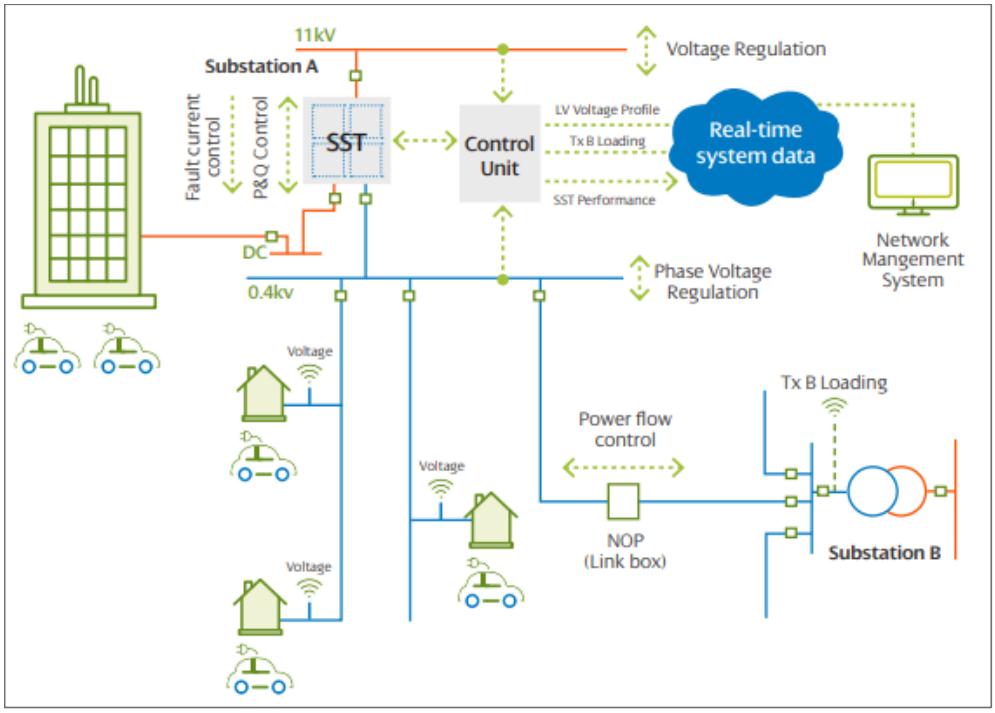


Figure 12 LV Engine project concept

As the focus of the LV Engine project is demonstrating the performance of the Core Functionalities required by the network, any innovative approaches that provide these Core Functionalities in an efficient and reliable manner was considered. Different possible SST topologies were explored of which two are described below:

- ***Topology 1*** - *Topology using a conventional low frequency 50Hz (LF) transformer* –This topology uses power electronics devices at the secondary side of conventional LF transformers (11kV/0.4kV). The power electronic devices can be added to the existing distribution transformers to deliver the Core Functionalities of LV Engine. SST Manufacturing Partner is required to provide the conventional transformer and the power electronic units. The aim is to enhance Technology Readiness Level (TRL) of this product from 6 to 9.
- ***Topology 2*** - *Topology using a High Frequency (HF) transformers* – Using HF Transformers and power electronics may allow a modular and compact design while delivering the LV Engine Core Functionalities. SPEN recognises that this topology will require a larger effort for design and manufacturing compared to the approach of retrofitting an LF transformer with power electronics. The aim is to enhance TRL of this product from 5 to 8.

3. SST Electrical High Level Building Block Design

The LV Engine SST design converts 3 phase delta 11kVL-L to 3 phase wye 400V L-L (230VL-N) and Vdc as shown in Figure 13.

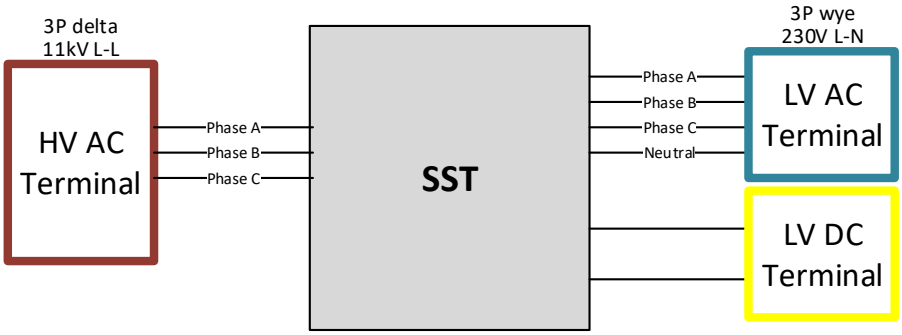


Figure 13 LV Engine Terminals

The use of power electronics allows for additional control beyond traditional voltage conversion. These features include those Core Functionalities defined in LV Engine project. The nominal system specifications for LV Engine SST are seen in Table 2.

Table 2 LV Engine SSTs Parameters

Nominal operating conditions	Requirements
Nominal power rating	500kVA
Nominal system frequency	50 Hz
System frequency range	47-52 Hz
HV network nominal voltage (RMS)	11kV L-L (6.4kV L-N)
HV voltage range	80-115%
HV nominal line current (RMS)	26A
HV unbalance voltage	3%
HV primary configuration	3 wire delta
LV network nominal voltage (RMS)	400V L-L (231V L-N)
LV voltage range	85-110%
LV nominal line current (RMS)	725A
LV unbalance load	0-100%
LV secondary AC configuration	4 wire wye
LV secondary DC voltage	±475Vdc
Vector group	DYn11

The high level system architecture initially considered for SST Topology 1 and SST Topology 2 are shown in Figure 14 to Figure 16. The components inside of the grey box indicate the components that EGB are responsible for design and manufacturing. The dotted lines indicate isolation barriers.

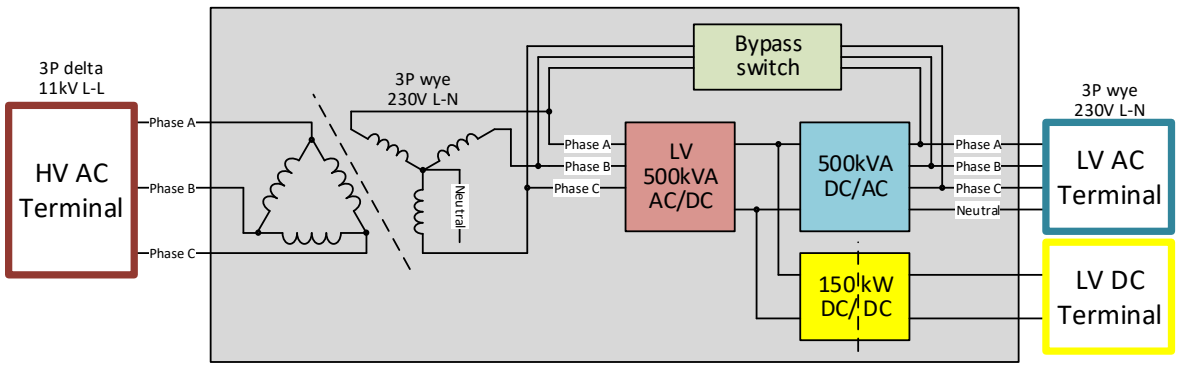


Figure 14 SST Topology 1 Block Diagram – Initial design considered

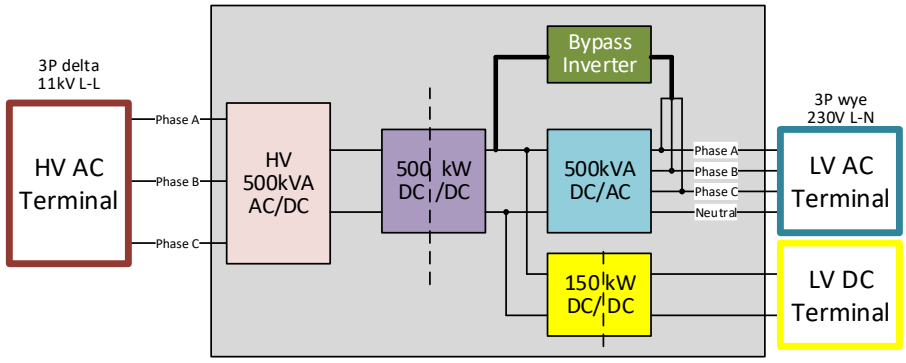


Figure 15 SST Topology 2 (type A) Block Diagram

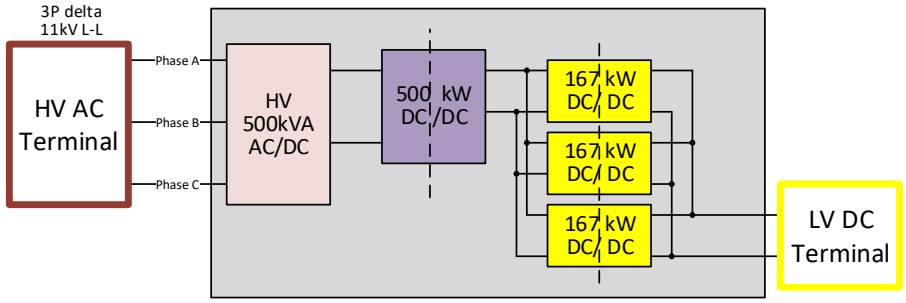


Figure 16 SST Topology 2 (type B) Block Diagram

This initially proposed system architecture was considered to be optimum as three designs share many similar building blocks, as shown in Table 3 below, including:

- The LV DC terminal of all three topologies is fed by the same DC/DC design; the higher 500kW power required in SST Topology 2 is attained by stacking three modules in parallel; and
- The LV AC terminal is also fed by the same inverter design in both SST Topologies.

The major difference between the SST Topology 1 and SST Topology 2 is the input 500kVA rectifier stage; the SST Topology 1 leverages a traditional transformer for isolation and stepping down the voltage while the SST Topology 2 must do this using two stages of power electronics.

Table 3 SST Building Blocks

	SST Topology 1	SST Topology 2 (Type A)	SST Topology 2 (Type B)
LV 500kVA AC/DC	✓		
HV 500kVA AC/DC		✓	✓
500kW DC/DC		✓	✓
500kVA DC/AC	✓	✓	
167kW DC/DC	✓	✓	✓✓✓

Although the initial design target was to use the above building blocks for the two SST Topologies, after further detailed design analysis, performance evaluation and mechanical design of SST Topology 1, it was decided to consider a Unified Power Flow Controller (UPFC) architecture for SST Topology 1 as shown in Figure 17.

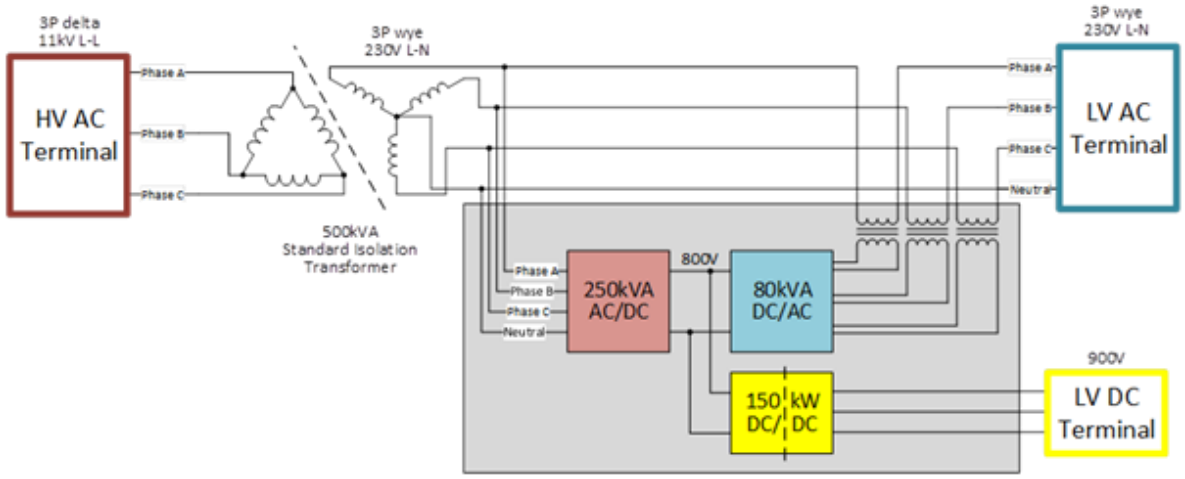


Figure 17 SST Topology 1, UPFC architecture

This decision was based on various product analysis carried out by the SST manufacturing partner and SPEN team with the aim to improve the reliability and adaptability of the product for business as usual deployment. Nonetheless, the detail of the initial SST Topology 1 design with the back to back arrangement has been published in Appendix A to ensure learnings from this design journey are properly disseminated as part of this deliverable. The main advantages of the UPFC (shown in Figure 17) over the back to back conversion architecture (Figure 14) are as follows:

- **Improved performance during the fault –** One of the main issues with the back to back converter is the limitation to provide adequate fault current to the faulted LV network so that the protection system can discriminate between normal load and fault current. The typical solution to this issue is to oversize the power electronics up to the minimum fault current requirement to operate the LV fuses (at least 315 A). However, by using the UPFC design the conventional transformer can contribute directly to the faulted network with the same level of fault current.
- **Improved efficiency –** The efficiency is expected to achieve the 99% efficiency if UPFC design is used as the power electronics do not need to supply all the LV demand and only operates to provide the system services. This will improve the efficiency and life-time losses significantly as the initial back to back design efficiency target was expected to be around 97%.
- **Smaller power electronics power rating –** Nominal power capability of the power electronics can be reduced significantly as the power electronics do not need to supply all the LV demand. In a back to back arrangement the power electronic must be rated at least 500kVA continuous loading, however the nominal power rating of the rectifier can be reduced to 250kVA in the UPFC design. This reduces the design complexity and also overall system cost.
- **Bypass capability –** The UPFC design provides bypassing the power electronic unit when it is not needed or if there is any issue with power electronic components. The bypassed capability can directly contribute to a better continuity of supply and reduce impact on customers.
- **Smaller dimensions –** The lower power electronics power rating, higher efficiency and capability to bypass during the fault conditions contribute to a more compact physical layout design compared to back to back design. The available space in a secondary substation is very limited therefore a compact design is desirable and practical for deployment.
- **Better reliabilities and building on previous EGB experience –** SST Topology 1 will be the first product of its type with no previous experience in the field, so the reliability of the product is yet to be seen in a live trial although reliability is seen in the design. EGB has existing 3 phase 150kW UPFC product which is currently commercially ready however this product does not deliver all the functionalities required in LV Engine and is not designed to UK standards.

4. LV Engine SST Topology 1

The principle design and operation of SST Topology 1 follows UPFC technology as the most versatile Flexible AC Transmission System (FACTS) device. SST Topology 1 consists of shunt power electronic units and series coupling transformers connected at the secondary side of distribution transformer. This topology can deliver desirable voltage set points (Magnitude and Angle) and also control the power flow.

The nominal system specifications for the LV Engine SST Topology 1 are outlined in Table 4.

Table 4 LV Engine ST Topology 1 nominal system specifications

Operating conditions	Specification	Notes
Nominal power rating	500kVA	Maximum rating
Nominal load current	725Arms	500kVA@230Vrms
Nominal system	50 Hz	-
Delta/Wye configuration	Wye in, Wye out	-
Operational modes	Radial or Mesh	V or I control
Nominal input voltage	249Vrms L-N	433Vrms L-L
Nominal output voltage	230Vrms L-N	400Vrms L-L
Operating temperature	-25C to +40C	
Imbalance control	30%	Max correction
Power Factor Control	0.893 to 1.0 PF	Max per phase
Output voltage control	38.6Vrms L-N	+ or – to input
DC Service @ +/- 475VDC	150kW Total	75kW per polarity

4.1 Block diagram summary

The Circuit Design incorporates an external 50Hz, 500kVA delta-wye transformer to step down the voltage from 11kV to 433V. This is done using SPEN's approved distribution transformer. After the HV to LV conversion, the power electronic circuit is utilised to perform the necessary power flow functions for the AC input and output.

The ST Topology 1 allows for the full 500kVA power to pass through the system while siphoning off a portion of power into the power electronics for processing.

A high-level block diagram of the SST Topology 1 showing all possible power flow is shown in Figure 18. In addition to the 500kVA 11kV/0.433kV transformer, the SST Topology 1 consists of four main components with specific functions described below.

1- **Rectifier (Rating = 250kVA)** –The rectifier's primary task is to draw power from the low voltage side of the 50Hz transformer to supply necessary power to the inverter and DC loads via a regulated 800V DC-link. Secondary purposes include supplying reactive power compensation and load imbalance cancelation seen by the distribution transformers.

2- **Inverter (Rating = 80 KVA**) – The inverter provides independent voltage and current control for each phase supplying the LV load. This is known as the series element as the inverter coupling transformer is in series with the source and load, allowing the inverter to adjust load voltage up to +/- 37V L-N with respect to the source voltage. In a mesh configuration the inverter can also operate in current control mode and send any combination of bidirectional PQ power (real and reactive current) given that the source and load voltage are within 37VL-N of each other.

3- **DC/DC converter (Rating = 150 KW**) – This is a fully isolated DC/DC converter providing bipolar ±475V DC with the ability to supply unbalanced LVDC load on each pole providing the loading on each pole does not exceed 75kW.
4- **Coupling transformers (Rating = 27kVA**) – Coupling transformers directly connected to the inverter block and setting up the voltage provided by the inverter to each phase independently.

Silicon Carbide (SiC) modules are utilised for all power conversion circuits to enable higher frequency operation and overall system size reduction.

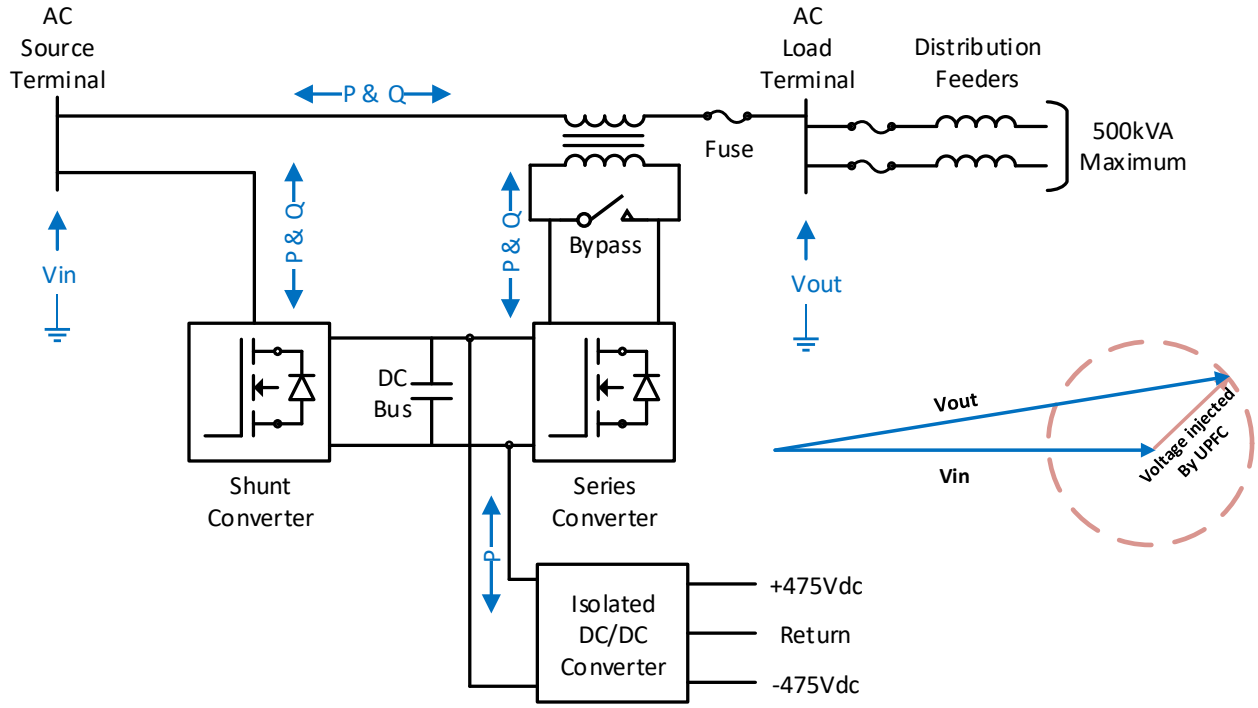


Figure 18 LV Engine SST Topology 1 Block Diagram

4.2 Power flow summary

SST Topology1 is able to operate in two different operating modes (Radial network and Mesh network). The operating mode will not be communicated to the unit in real-time, thus additional built-in controls (discussed in B.3) are required for detection to facilitate correct operation and protection.

1- **Radial network:** In a radial network the SST becomes an LV voltage source, acting in voltage control mode at a specified set point.

2- **Mesh network:** In a mesh network SST operates in a combination of the voltage control and power control modes to hit a P, Q target set point while ensuring the voltage remains stable. This is further discussed and demonstrated in Appendix B.

An optional DC Service Port provides a fully isolated and power limited +/- 475Vdc output up to 150kW.

4.3 System Architecture

The high-level 3-Phase 500kVA system architecture for the SST Topology 1 is shown in Figure 19. The components inside of the grey box indicate the power electronics system which will be added to the conventional distribution transformer, the light green boxes indicate existing equipment at the substation:

- A 4-leg half-bridge 250kVA shunt converter provides power for the Series Inverters, Imbalance control, Power factor correction and DC Service functions within the SST.

- Three full-bridge 30kVA series converters (labelled A, B and C) provide the necessary power via the 27kVA coupling transformers for voltage control in Radial mode and P & Q power control in Mesh mode.
- The 150kW DC-DC converter is a factory ordered option to provide a fully isolated 3-wire +/- 475Vdc Service Port.

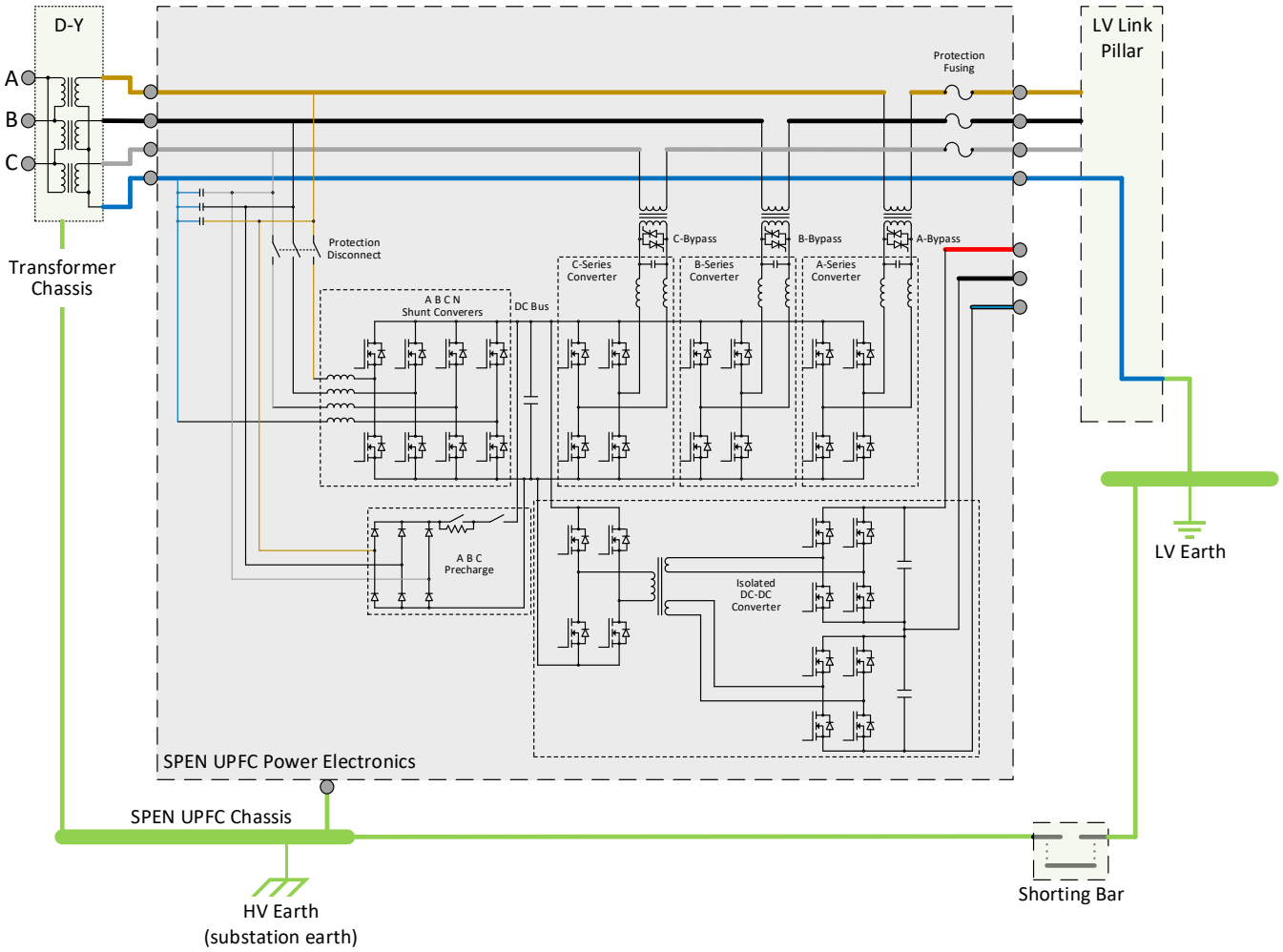


Figure 19 SST Topology 1 System Architecture

4.3.1 Earth, Bonding and Grounding

The compliance with SPEN's earthing and bounding policy[1] needs to be considered in SST design. HV and LV Earth are required to be separate with a shorting bar within the LV Link Pillar providing HV to LV Earth bonding when deemed permissible by SPEN, during the substation installation and commissioning procedures.

A diagram of the SPEN Secondary Substation Earth Design that illustrates these guidelines is shown in Figure 20. The LV Neutral is bussed straight through the SST Topology 1 and is not internally tied to the power electronic box chassis. All metallic surfaces including the power electronic box within the substation are bonded to the HV earth (if not a high EPR site) for enhanced operator safety.

[1] Technical specification for earthing and bonding at secondary substations, available @ https://www.spenergynetworks.co.uk/userfiles/file/EART-03-003.pdf

The main reason that LV Neutral is passed through the power electronic box is for sensing purposes to accurately and reliably control imbalance load seen by the Transformer as one of the core requirements of the SST Topology 1.

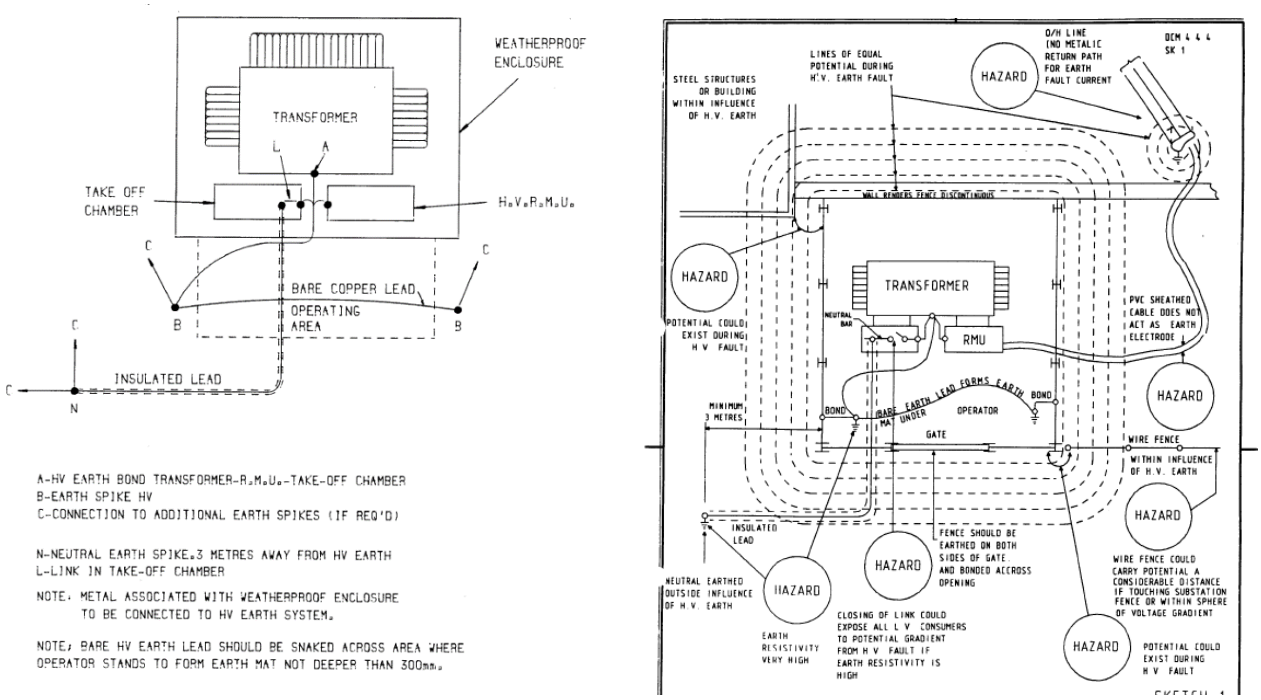


Figure 20 SPEN Secondary Substation Earth Design

4.3.2 250 kVA Rectifier requirements and design

The nominal operating conditions of the rectifier is shown in Table 5. These values drive the selection of hardware components for the rectifier.

Table 5 general specifications of rectifier

Operating conditions	Specification	Notes
Nominal power rating	250 kVA	
Nominal system frequency	50Hz	Normal operating range 47-52 Hz
Nominal Voltage	433 L-L (250 L-N)	
Nominal current	360A	

The rectifier topology consists of a traditional 2-level 3 phase inverter circuit with an extra 4th half bridge phase for neutral compensation. The 4th half bridge phase cancels out the sensed load neutral currents (up to the current limits of the hardware) to minimise neutral current that is fed back to the delta-wye input transformer.

SiC modules from various manufacturers were considered and analysed for best system fit, the detail of this analysis has been shared with SPEN but cannot be published in this document due to commercial sensitivity. Various device parameters such as parasitic capacitance, gate threshold, stray inductance, body diode characteristics, and gate charge were evaluated. The top priority is that the modules need to operate reliably which means the following criteria were set as the priorities:

- Available thermal headroom for junction temperature;
- Provisions for short circuit protection;
- Optimal mechanical packaging for isolation requirements and thermal management.

Thermal analysis was done by modelling each device's thermal and electrical characteristics in PSIM and calculating power loss and junction temperature of a device in a working circuit. This helped EGB provide a similar comparison across device characteristics and manufacturers. For EGB's analysis, the case temperature and junction temperature were fixed at specific values and the resulting current the device could handle was recorded as the result.

Based on the SiC modules selected for the rectifier, at 360A of current for each phase, or the full 250kW rating, the half bridge arrangement will dissipate roughly 1192W. With four half bridges running at full current the total power dissipation is 4768W. Switching loss accounts for approximately 78% of total device losses at full load (250kVA).

4.3.3 80 kVA inverter

The power rating of the inverter is calculated as follows:

- the load current is nominally 725A and the inverter will correct up to +/-37V, so each inverter phase will provide 725A*37V = 26.8kVA. Thus all 3 full bridges together will be rated at 26.8kVA*3 = 80kVA**.**

Table 6 General Specification of the 80kVA Inverter

Operating conditions	Specification	Notes
Nominal power rating	80 kVA	
Nominal system frequency	50Hz	Normal operating range 47-52 Hz
Nominal Voltage	450 L-L (250 L-N)	
Nominal current	60A	

A basic diagram of how the series element adjusts output voltage is illustrated below in Figure 21. The inverter essentially becomes a series voltage source in line with the source and load.

As an example, one can examine a hypothetical radial network where the source voltage is 233V and the customer desires 270V on the loads. In this scenario, the secondary side of the transformer would need to add 36.8V to achieve 270V. The 37V across the secondary of the transformer translates to the inverter outputting 37V*12=444V. If buck operation is desired, the inverter simply reverses its output phase.

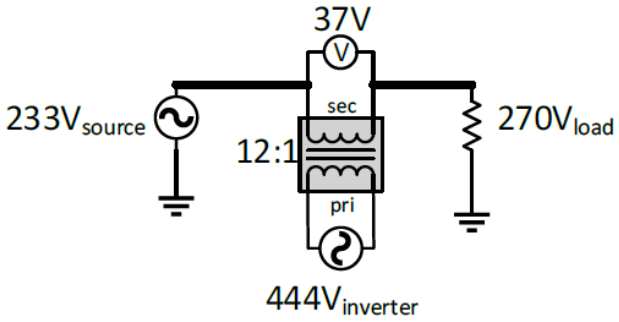


Figure 21 Voltage Buck/boost principle of series inverter in radial network

When the ST operates in an LV interconnected arrangement for capacity sharing with another substation, the inverter will operate in current control mode. Using Figure 22 as a reference, if a 300A of load current set point is sent to the SST Topology 1, the inverter will control its output to achieve the desired 300A towards the load. The 12:1 transformer converts the 300A from the secondary winding to 25A on the primary. Just as with a radial network, if it is desired to send 300A in reverse (from load to source), then the inverter simply reverses its output phase.

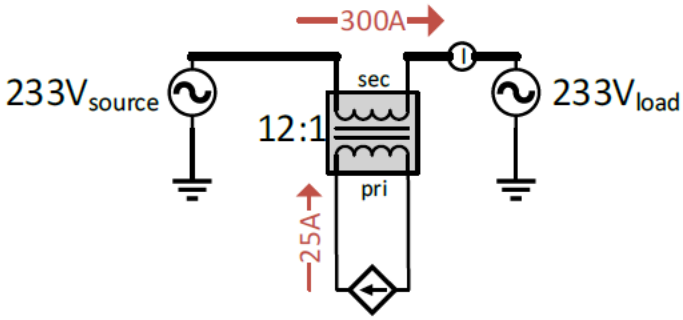


Figure 22 Current Control of Series Inverter in Mesh Network

Two topologies were discussed for the inverter: i) a traditional half bridge topology versus ii) a full bridge for each phase, seen in Figure 23. The full bridge was chosen as each phase is truly independent of one another; there is not a common return path (as seen in the half bridge). The downside with the full bridge is that 2 additional half bridge modules are required, but other benefits outweigh this drawback:

- To achieve the same power output, the half bridge requires twice as much current since it can only output half the voltage of the full bridge. Thus, device and magnetics stresses are reduced in the full bridge.
- The equivalent switching ripple seen by the inductors in the full bridge is twice the switching frequency. The combination of the switching ripple benefit and lower current reduces inductor size in the full bridge topology.

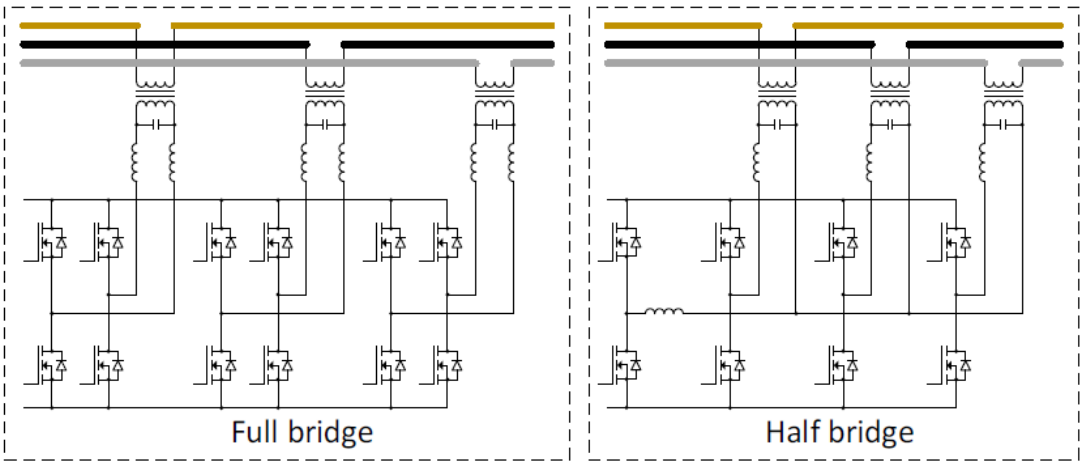


Figure 23 Full bridge vs Half Bridge Inverter Topologies

Compared to the rectifier devices, the inverter devices experience significantly less power dissipation due to the inverter current being 1/6 of rectifier current. Therefore, the rectifier drives device selection while the inverter devices need to be lower current and compatible with the rectifier devices. Similar to rectifier, market research and devices assessment carried out to select the SiC devices for the inverter, the sensitive commercial and market research information has been shared with SPEN.

Based on the final selection, the SiC device loss for each full bridge is 212W, for a total of 636W of device losses from the inverter section. The full bridge can handle 247A which is more than the 60A requirement of the inverter. Although the efficiency is lower than half-bridge, but the LV Engine project team agreed that thermal capability headroom is more important at this stage of product development to ensure higher reliability which is an acceptable trade-off.

4.3.4 Coupling transformer

The transformer is specified to handle 27kVA with a 12:1 turns ratio (450V to 37V). The product is selected based on the existing market knowledge EGB has on single phase transformers and building on the knowledge gathered through their GER developments. The selected single phase transformer will be approximately 381mm x 330mm x 300mm (WxDxH) and weigh 200kg. There will be three transformers for each series inverter.

The special consideration for the coupling transformer in LV Engine is that it needs to handle the short burst of high energy during a downstream fuse clearing event, LV feeder fault. The secondary winding of the transformer handles 725A nominally however the much larger fault current can be expected therefore a protection strategy detailed out in Section 4.5 has been considered to ensure the unit is adequately protected in any fault event.

4.3.5 150kW DC service

The DC service requirements are listed in Table 7.

Table 7 DC Service Port Specifications

Operating Condition	Specification	Notes
DC Input Voltage	800 VDC	From DC link of a low voltage 3-phase
DC Output Voltage	±475/950 VDC	Bipolar/Unipolar output
DC Output Current	526 (158) ADC	Maximum continuous rating @ 950VDC
DC Output Power	500 (150) kW	Maximum continuous rating, 250 (75) kW
DC Voltage Ripple	±20Vmax	0-400Hz
Voltage Tolerance	0.5%	Bipolar/Unipolar output
Max Voltage Mismatch	5V	For bipolar application only
DC Dynamic Regulation	<20V	Slew rate of 200A/second
Over Current Protection	556 (167) ADC	Constant Current Mode before UV
Over Voltage Protection	1000V	Instantaneously
Under Voltage Protection	850V	Instantaneously
DC Earthing	To Chassis	For bipolar configuration, the earthing

The DC/DC topology is proposed to be a phase shift triple active bridge (TAB) converter, derived from the popular dual active bridge (DAB). The TAB allows for a wide range of voltage control on the output and can seamlessly transition between positive and negative power flow. As the TAB is an isolated DC/DC, tying the DC/DC common terminal to ground potential has no impact on rectifier and inverter operation as the isolation barrier allows the internal DC-link to float as needed.

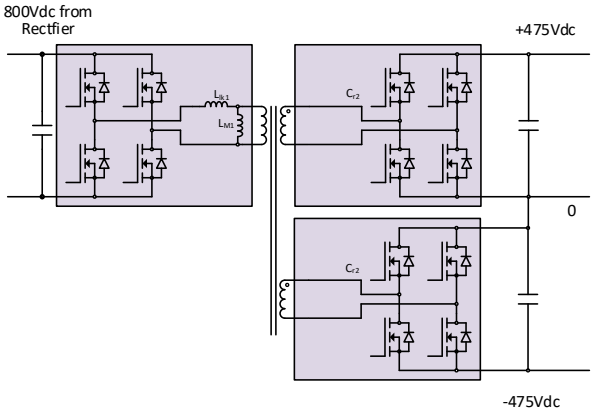


Figure 24 TAB DC/DC setup for 167kW

The primary consideration for the design of the TAB is to ensure zero voltage switching (ZVS) of the SiC modules throughout the entire operating range. Transformer leakage inductance is the key parameter in achieving ZVS. The higher the leakage inductance the wider the ZVS range, but higher leakage inductance also leads to higher RMS currents and higher overall conduction losses. Higher leakage inductance also means greater phase shift is needed to provide the same gain; phase shifts greater than 30° start to exhibit nonlinear behaviour and are harder to control. As a result, there is a careful balancing act to design the TAB for ZVS while also managing efficiency and stability.

In order to streamline the supply chain and mechanical design, the DC/DC shares the same SiC modules as the rectifier and inverter. The transformer has a special “pdqb” winding method. The pdpq winding method describes an interleaved edge-wound winding which allows for precise control of transformer leakage inductance, critical for ZVS performance. The technical details of the components and suppliers have been shared with SPEN in confidential documents.

The output capacitor must be designed to handle the ripple which impacts the output voltage specification. Based on information gathered from the EV charger manufacturer, the output capacitor is chosen to keep the output voltage under 20Vmax ripple, 10V preferable.

Figure 25 shows that the output capacitor is required to suppress the high frequency noises brought by the switching frequency related sources. To meet the specification of EV charger manufacturer, specially the DC dynamic requirement of sudden shutdown without notice, approximately 900uF output capacitance is chosen per 167kW.

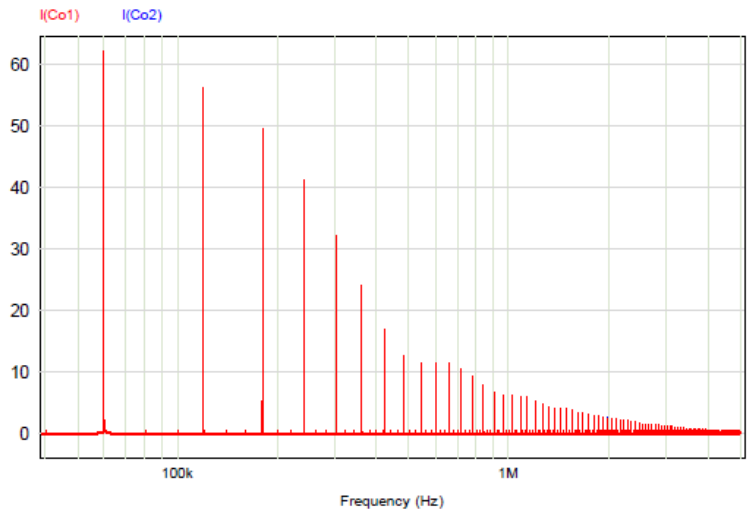


Figure 25 20 Ripple FFT on Output Capacitor

4.4 Insulation and Isolation

The conventional delta wye transformer provides the required HV-LV isolation for the substation equipment including the power electronic unit at LV. The equipment isolation requirement for the power electronic unit (as required by IEC 60076-3) is 3kVrms at 50Hz for 1 minute as shown in the first row of Table 8.

As a design objective, EGB is targeting isolation at 4.0kVrms @ 50Hz for 1 minute for internal components requiring isolation to the metallic chassis. This aim allows a design margin to this important operator safety requirement.

Table 8 Insulation & Isolation Requirements Table from IEC 60076-3

Highest voltage for equipment (kV r.m.s)	Nominal voltage (kV)	Rated lightning impulse voltage (LI) (kV Peak)	50 Hz withstand voltage (kV r.m.s)
1.1	0.40/0.23	-	3.0
7.2	6.6	60.0	20.0
12.0	11.0	75.0	28.0

4.5 Protection Hardware – Core Functions

There are multiple core functions required for the SST Topology 1 protection hardware. While there are many additional control firmware and management software protections built into the design, this section addresses the core functions of the primary protection hardware as summarised in the points below:

1) Protect the UPFC from damage during **external** overcurrent/fault events including:
   - Load overcurrent events – Cold load pick up
   - Source or Load overvoltage
   - Any fault in LV feeders
   - Any fault within the substation between SST Topology 1 exit terminal and the LV board

2) Protect the UPFC from potential damage during **internal** faults:
   - Shunt Converter over-current event
   - Series Converter over-power event
   - Any unexpected fault on fixing, joints, busbars etc

Figure 26 shows the protection equipment that will be used within the hardware design of SST Topology 1.

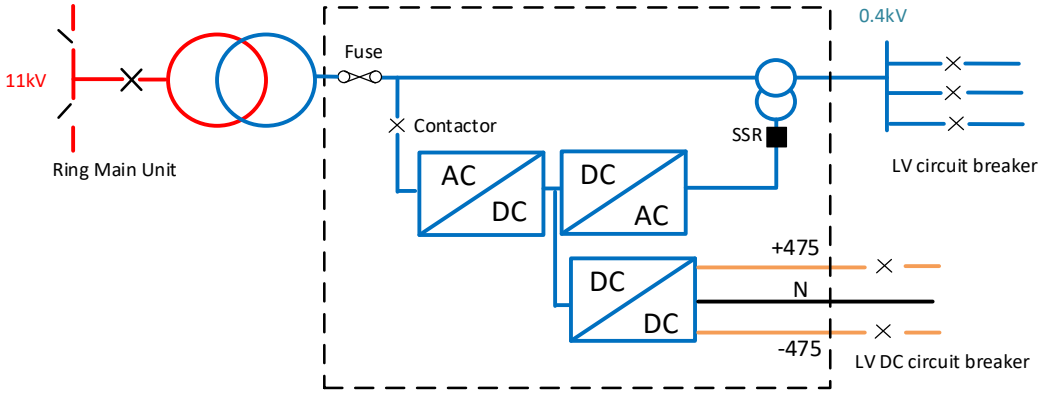


Figure 26 Protection Hardware considered in SST Topology 1 design

4.5.1 Protection during External Faults

The following external fault conditions for which the SST Topology 1 is specifically engineered to handle with measurement, detection and appropriate real-time actions:

- **Load overcurrent** events are reliably detected, and SST autonomously reverts to Bypass mode from Operational mode, as required. This is implemented with a Solid-State Relay (SSR) on the Inverter side of the coupling transformer. Further details are given in 4.5.3.

- **Source overvoltage or Load overvoltage (in Mesh mode)** events are reliably detected and the SST autonomously reverts to Bypass mode as explained above. If the overvoltage level is deemed as potentially harmful to the Shunt Converter, the Shunt Converter disconnect switches will be activated, disconnecting the Shunt Converter from the Source terminals. LV network supply will be maintained through direct connection to the transformer. The system will autonomously recover normal operation after the fault condition subsides.
- **Fault at LV feeders** are reliably detected, and the ST autonomously reverts to Bypass mode from Operational mode by closing SSR. The primary protection for any fault clearance in LV network is by using LV CBs.
- **Fault in LV small zone** – Any fault within the substation between SST exit terminal and the LV board. In a conventional substation arrangement, any fault in this area should be cleared by the HV switchgear i.e. RMU. With SST integrated, for any fault in this area the following strategy will be implemented:
    - An 800A user serviceable fuse in series with the SST input and output bushings and through the coupling transformer. This fuse rating is coordinated with the SSR rating to protect the SSR while protecting the whole unit.
    - Issue a 24V tripping signal to shunt tripping coil in Ring Main Unit; the circuit breaker will open and, as a result, the substation is disconnected from HV. This operation is expected to take around 100ms after the hardware signal goes active.

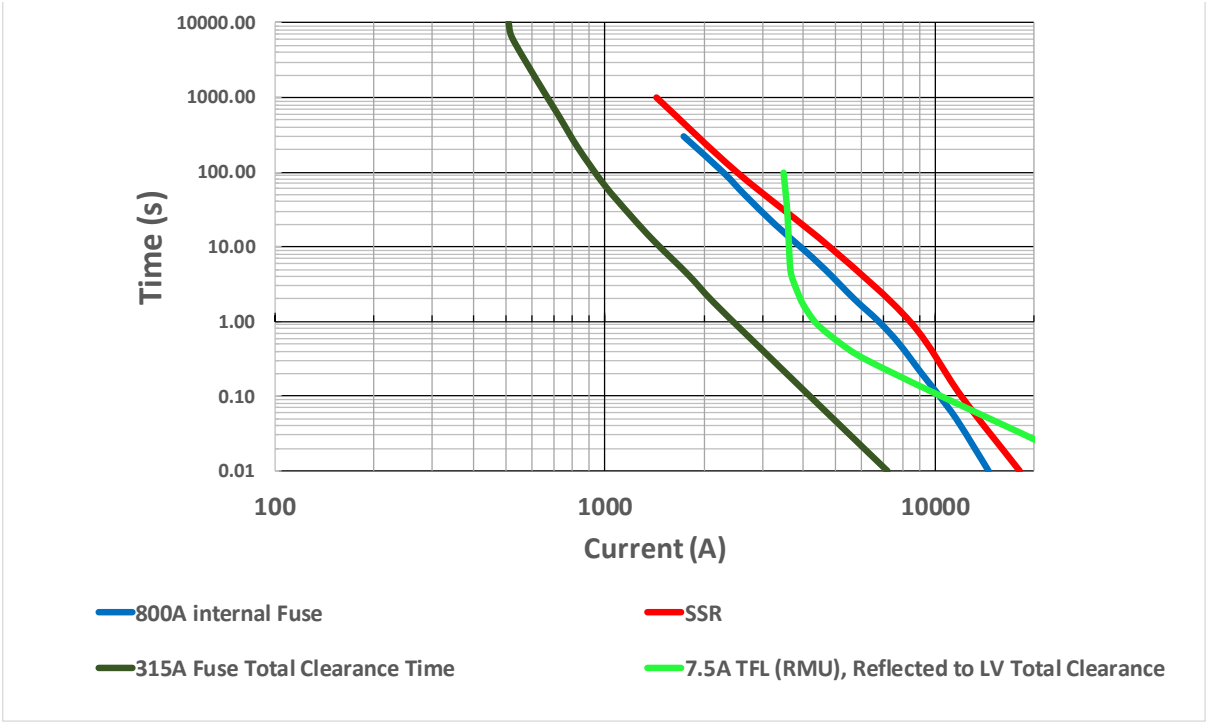


Figure 27 SST Topology 1 protection coordination

4.5.2 Protection from Unexpected Internal SST Faults

The following protection strategy has been considered for internal faults:

- **Shunt Converter over-current event:** The shunt converter will be protected from both over current and over voltage with internal sensors, controls and disconnect switches to protect and shut-down the power electronics.

- **Series Converter over-power event:** The series converter will be protected from both over current and over voltage with internal sensors and proper controls to protect and shut-down the power electronics. The SSR can be utilised to protect the series converter from excessive voltage across the SST Source and Load bushings which would be reflected across the coupling transformer as a higher voltage, potentially damaging the series converter power electronics.

4.5.3 Bypass Solid State Relay

The function of the SSR is crucial in the overall protection and operation of SST Topology 1. The design includes three separate SSR modules for each inverter, see Figure 28.

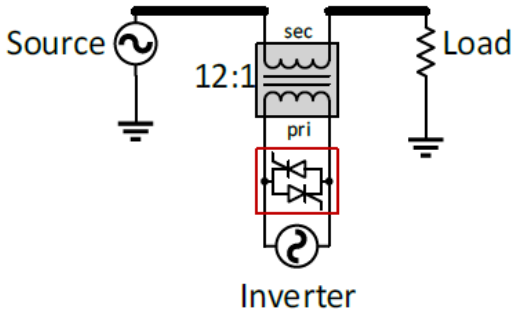


Figure 28 SSR situated in the secondary side of coupling transformers

The SSR serves the following purposes in the system:

- Bypass the power electronics during fault, start-up scenarios or any other operational scenarios; and
- Force coupling transformer windings to 0V protecting from any overvoltage passes to the converter
- Allow operation staff to locally bypass all the power electronic operations if required

The SSR closes whenever the unit enters bypass mode. Bypass is defined as “the state in which the SiC devices are off and the source passes directly to the load; protecting/bypassing the power electronics while still providing power for downstream loads”. The definition of Bypass is the same in both radial and mesh networks.

When the SSR is closed, the primary windings of the coupling transformer will be forced to 0V, which is reflected to the secondary side as a short, also forcing the secondary windings to 0V. Without this feature, a large load current would create a voltage drop across the secondary of the transformer which then reflects by the 12:1 ratio to the primary windings - This induced voltage could be potentially damaging to hardware.

With these purposes in mind, the SSR needs to meet the following design objectives:

- Exceed the time vs current or I^2t energy rating of the downstream fuse target capability
- Be normally closed to prevent reflected voltage during start-up

The SSR will be built with back to back thyristors to form an AC switch. The thyristors will be sized such that when they are closed during bypass, they can handle the energy required to trip a downstream fuse (315 A) while also providing for static loads. EGB design, build and test the SSR internally.

4.6 Voltage operation range

SST Topology 1 provides 36.8V (16% nominal rating, 230V) voltage boost/buck for each phase separately. This voltage regulation can be delivered within ±15% deviation from input nominal voltage (0.4kV L-L). It is important to understand how all the various voltage ratings relate to each other when

SST operates during normal and abnormal conditions. Table 9 and Figure 29 show the key voltage specifications for operation.

Table 9 Voltage Summary Table – Line to Neutral

Voltage Condition/Range	Specification	Notes
Input Line to Neutral Range	230Vrms +15%, -15%	
Output Line to Neutral Range	230Vrms +10%, -6%	
Buck-Boost Range, Source to Load	36.8Vrms or 16%	From 230V nominal
500kVA Transformer output nominal	250Vrms	+8.25% of 230V
System Start-up Range	+ 13%, -13%	2% hysteresis from
System Regulation Range	+15%, -15%	
Ride-thru & Fault Voltage Range	+18%, -18% for 3 Sec.	Before Bypass

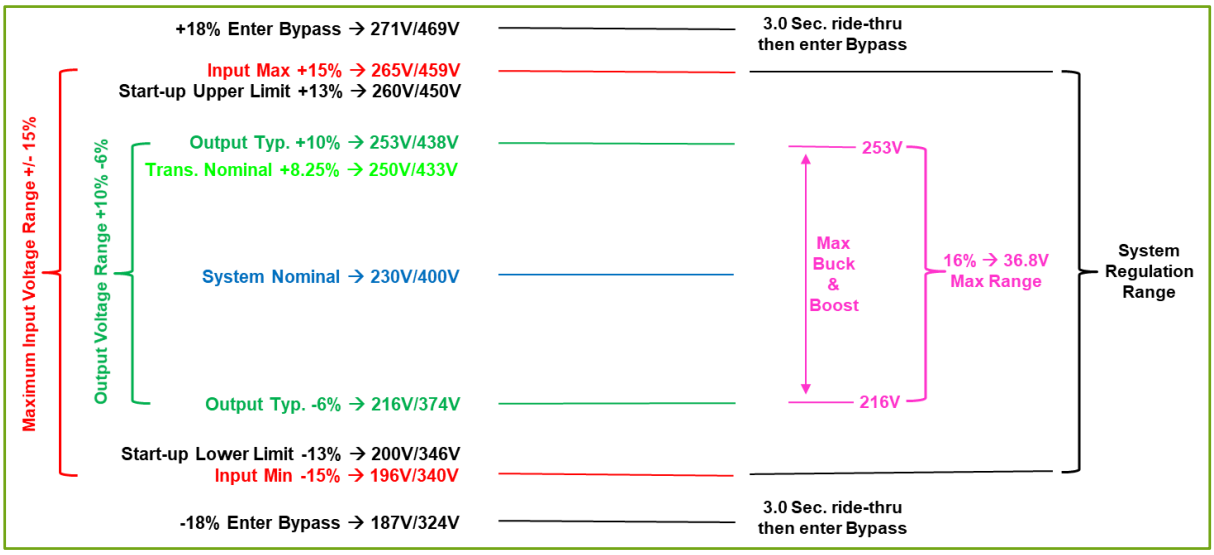


Figure 29 Voltage Summary Chart

4.7 Operation modes

4.7.1 Radial and meshed operation mode

In order to deliver the LV Engine Core Functionalities, SST may operate in a radial or interconnected LV network arrangement. In an interconnected LV network, SST may control the power flow within the interconnection following the control power command received from SCS. The SST power flow control strategy shall include the following network conditions and issues:

1- Unexpected change in LV network from radial to an interconnected arrangement should not cause any interruption or issue in SST operation or cause rapid voltage step change at LV (or HV). This may happen as the status of Normally Open Point within LV networks may be altered by operation staff inadvertently forming an interconnected or radial network.

2- In case of sudden change in load e.g. losing an LV feeder, the voltage should stay stable as any rapid voltage change should be within the limits specified in IEC 50160.

3- The control system should account for delay in communication and update on the status of interconnection to the SST, i.e. the SST may be updated on the status after a couple of minutes (depends on the comms) of actual change taking place.

In order to address the aforementioned concerns and ensure that the LV voltage at the secondary substation remain stable in the event of network reconfiguration or loss of loads, after extensive desktop

studies considering different network scenarios, the control strategy illustrated in Figure 30 will be implemented:

1- In a radial arrangement SST controls LV voltage based on the Voltage setpoint commands received from SCS.

2- If any power flow command received by SCS, SST change the control to Power Control mode and adjust the voltage (magnitude and angle) at the LV terminal to achieve the P & Q set points. Due to very regular variations of the load in the LV networks, rather than fixed values for P&Q set points a range of acceptable P&Q command will be sent to SST.

3- If the P&Q supplied by the SST is within the range of the P&Q set point commands, SST switches back to voltage control mode and maintain the voltage (magnitude and angle) at the level which satisfied the P &Q command.

4- The P&Q supplied by SST will be constantly monitored. If the monitored values go outside the P&Q command range it will inform SCS that the P&Q is out of range now, however, no adjustment to P&Q will be conducted. This may occur as a result of natural change in LV demand.

5- If a new set of P&Q commands are received, SST starts the Power Control mode again to satisfy the P&Q command and then switch back to Voltage Control Mode.

6- When operating in either Voltage Control mode or Power Control mode, SST will maintain the voltage at LV terminal within a configurable permissible range.

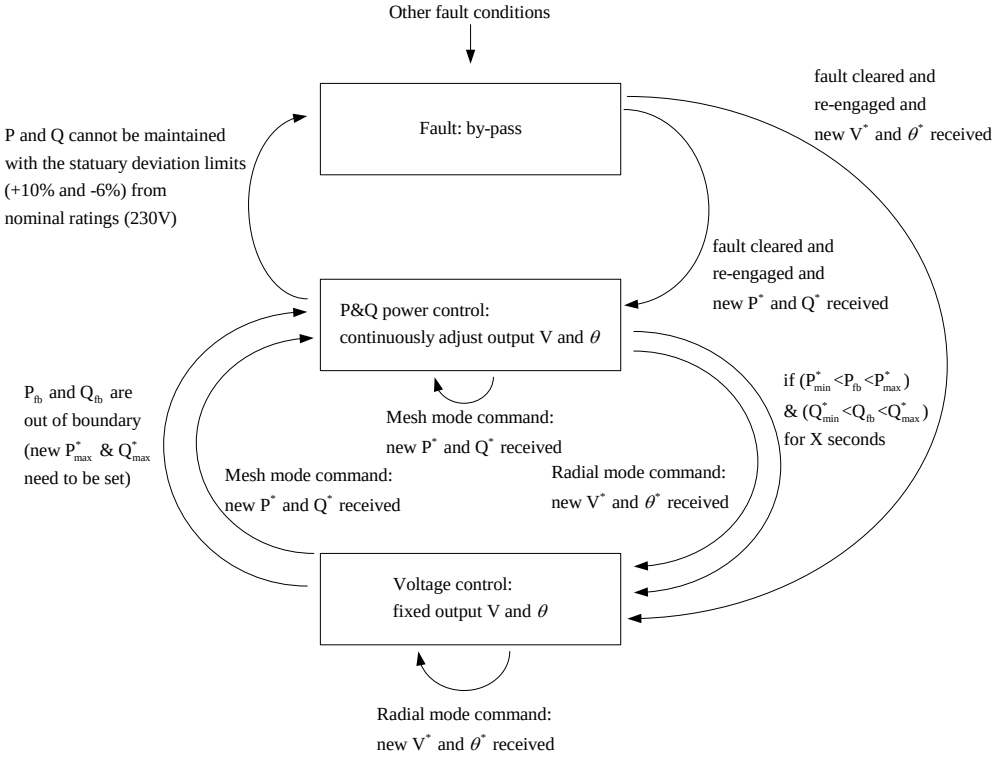


Figure 30 Control strategy during meshed and radial network arrangement

4.7.2 DC operation mode

DC supplied EV charger units, manufactured by Tritium, will be used in the LV Engine trial. There are ongoing communications with Tritium to detail out the requirements and interfaces.

The EV charger will behave as a constant power load. Though a fixed bipolar arrangement, ±475V is provided when the total amount of load power is within 500kW (150kW), the output voltage will deviate

from 950V in cases of overloading or transient conditions. Constant power and constant current mode operation are provided by the DC Service Port to avoid the unnecessary blackout in overloaded or transient cases, shown in Figure 31.

The DC Service Port will operate at constant power mode of 500kW (150kW) when the voltage at the output terminal at its 950V nominal or within the allowable range from 900V to 1000V. When the output voltage drops below 900V, the DC Service Port will operate at constant current mode of 556A (167A) before the undervoltage protection is triggered at 850V. The current strategy is to allow a 1.0 second 167A overload period in the 150kW model in constant current mode to allow EVs and their Chargers time to shed power using their existing communication protocol. However, this overload capability will not be available in the 500kW model.

The overall DC system will benefit from the proposed operation modes in light overload cases:

- Constant power mode will improve the power deficit if other types of loads (constant impedance/constant current) are connected to the DC bus. The output voltage may stop falling if the load power returns to 500kW (150kW) and resumes power balance.

- The constant power and constant current modes could effectively increase the allowable action time for the Tritium EV Charger to cut off its connected EV load when it is overloaded, avoiding the unnecessary blackout especially in light overloaded case.

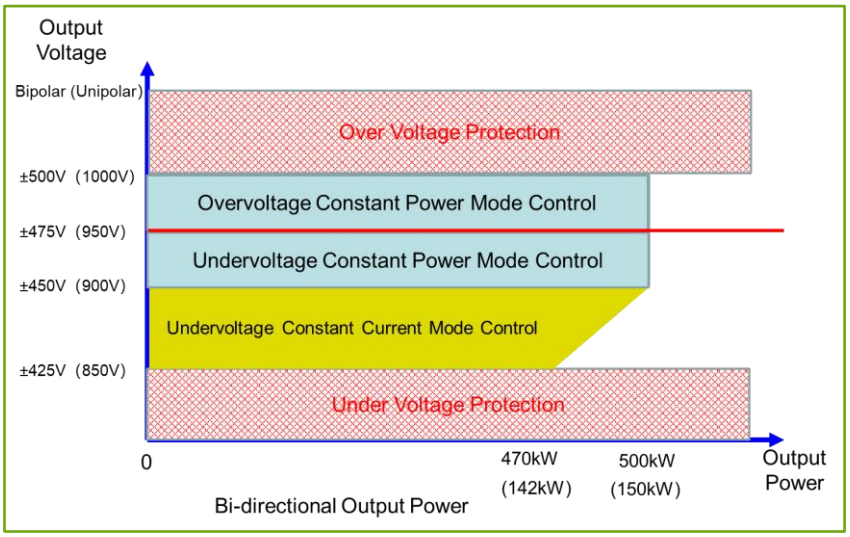


Figure 31 DC Service Port Operational Modes

Considering the variation of EV user charging behaviour and potentially long idle time of the charger, the efficiency at full load range should be high. Hardware optimization and control strategies have been developed by EGB team which provides a fixed 950V output at all times with high efficiency with no actions required from the load side.

4.7.3 Service priority

It is unlikely that all the Core Functionalities are required simultaneously at full 500kVA loading condition. This is a practical assumption made to avoid overdesigning the unit which may not be required in a real field application. Instead, in an unlikely operation scenario, when SST reaches its permissible thermal, power or current rating, some of the services namely Imbalance load cancelation and power factor correction will be gracefully degraded. Table 10 shows the service priorities will be set in the ST control strategy to degrade the services if required.

Table 10 Services degradation in case ST reaches its thermal rating

Priority	Total load	Total Imbalance cancelation	PF target	Voltage control (boost/buck)	DC
1	500kVA	30%	Unity	36.8V	150kW
2	500kVA	20%	Unity	36.8V	150kW
3	500kVA	10%	Unity	36.8V	150kW
4	500kVA	0.0%	Unity	36.8V	150kW
5	500kVA	0.0%	Load PF	36.8V	150kW

4.8 Mechanical design

The SST Topology 1 mechanical packaging will be confined to a 1.5m^3 overall envelope size including all required cooling apparatus and cable boxes. This is a target design and is being finalised with the aim to include the factory ordered optional 150kW DC Service Module in the target envelope size. The latest layout design is shown in Figure 32. The design process was initiated through the Project Inception phase, where regular detailed discussions with the SPEN team were held to translate each of the technical/functional requirements specified within the Smart Transformer Technical Specifications.

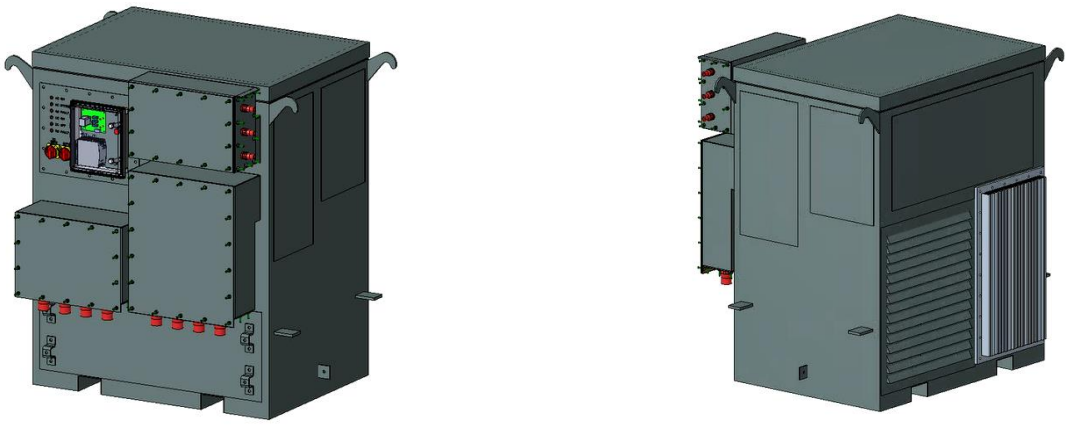


Figure 32 Latest Mechanical Design – Front & back views

4.9 SST Topology 1 Thermal Management

Thermal Management is a critical function for long term reliability of any power electronics design. Due to the high-power requirements, the 500kVA ST will require two modes of active cooling to provide sufficient operational margin of at least 20°C for critical components. This margin will be actively monitored, and the system performance will be systematically reduced (see section 4.7.3) or will revert to Bypass as a last step to thermal protection. The two mode of active cooling are as follows:

1- **Active liquid cooling** in the form of cold-plates (as shown in Figure 33) for the SiC modules, SSR Thyristors, DC-DC Transformer, and the high-current shunt converter inductors. These are the highest power dissipating devices within the overall design. The liquid coolant will dissipate its heat into the ambient environment using a water-to-air heat exchanger, functionally similar to an automotive radiator. This system will require no annual maintenance once put into service. The design goal of this closed-loop system is to provide 65°C liquid coolant to the input (cool side) of the cold-plates. Preliminary heat-load estimates for a fully operational AC & DC

system are shown in Table 11. It should be noted that the total heat loads at the bottom of this table will never be realized. This total represents each component operating at its maximum capacity simultaneously. The estimate is that the total efficiency will be ~ 99% at full load.

2- **Active air-cooling** implemented as an internal circulation fan that will move concentrated and stagnated heat from lower-power components/devices to the outer walls of the enclosure that are exposed to the cooler ambient air, keeping the internal air temperature at 70°C or lower. This will provide 15°C of operational margin for 85°C industrial rated components.

Table 11 Preliminary estimate on MAX SST Topology 1 Heat Loads

Device/Component	Heat Load (W)	Qty.	Total Heat Load	Notes
SiC Modules-Shunt	1400	3	4200	20kHz Fs, 65C Case
SiC Modules-Series	212	3	636	20kHz Fs, 65C Case
SiC Modules-DC HB	450	2	900	30kHz Fs, 65C Case
SiC Modules-DC-FB	290	4	1160	30kHz Fs, 65C Case
Shunt Conv. Inductors	350	4	1400	Supplier calculation, Max
Series Conv. Inductors	50	6	300	Estimate, Max
SSR Thyristor SS	85	3	255	980Arms Bypass, Steady State @1V
SSR Thyristor Peak (3Sec)	167	3	501	To clear series fuse. (est. 2kArms @1V)
Coupling Transformers	108	3	324	99.6% efficient
DC-DC Transformer	850	1	850	Calc. Max from muRata
System Power Supply	24	1	24	95% efficient, 480W
SiCSM	15	2	30	Estimate, 2nd for DC Service
System Conduction Loss	250	1	250	0.05% Est. @ 500,000
Other System Losses	250	1	250	DC Link, AC Caps, Etc
			10,579	**Total - Continuous max losses (97.9% efficiency)**
			7,669	**AC Total – continuous max losses (98.5%)**

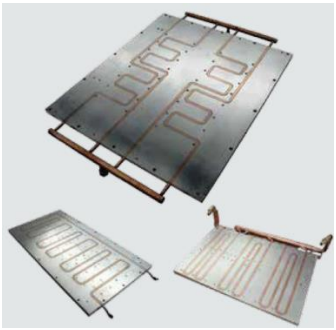


Figure 33 Typical Cold Plate used when cooling high-power electronics

As a potential engineering improvement for a possible second generation of the SST Topology 1 implementation, the water-to-air heat exchanger could be replaced with a passive radiation system. Active liquid circulation would remain a critical component of this implementation for safe operation and operating margins. The feasibility of this potential improvement will require actual thermal data from field deployments operating in Radial, Mesh and DC Service installations which will be part of LV Engine site trial delivery.

4.10 SST Topology 1 Local Interface

The local SST interface shown in Figure 34 aims to provide the following main functions:

- Providing indicators confirming the operation status
- Access to switches providing the option for the local operation staff to switch off/on the power electronics that includes bypassing the AC services and coupling transformer, and switching off the DC operation
- Connection to the Ethernet port for communication with SPEN telecoms/router with which communicating control commands, monitored parameters and remote access is facilitated.
- Access to auxiliary power supply providing 24DC for HV switchgear inter-tripping scheme and supply for the telecoms with secondary substation
- Access to the contactor relay for connection of the 24VDC to HV switchgear's shunt trip coil.
- Provide a test point (via a multi-meter device) for the operation staff to ensure no internal capacitor charge exists before any work on the device.

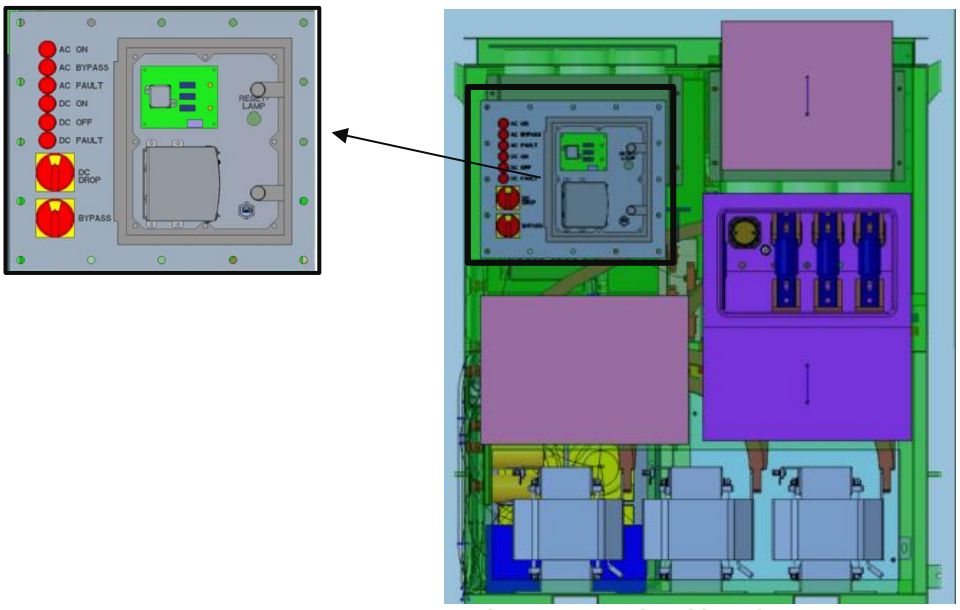


Figure 34 SST local interface

All the switches will be padlockable allowing only authorised operation staff to conduct the switching actions. The auxiliary power supply, serial port and contact relays will be also housed in a padlockable enclosure.

5. LV Engine ST Topology 2

The following section provides the outcome of design work carried out for the SST Topology 2 design. It should be mentioned that some the detailed design presented in this section may change as a result of ongoing engagements with suppliers and prototype works.

SST Topology 2 consist of three stages the HV AC/DC stage, DC/DC stage and DC/AC stage. The overall building block of SST Topology 2 is shown in Figure 35. The designs considered in each stage are explained in the following Sections.

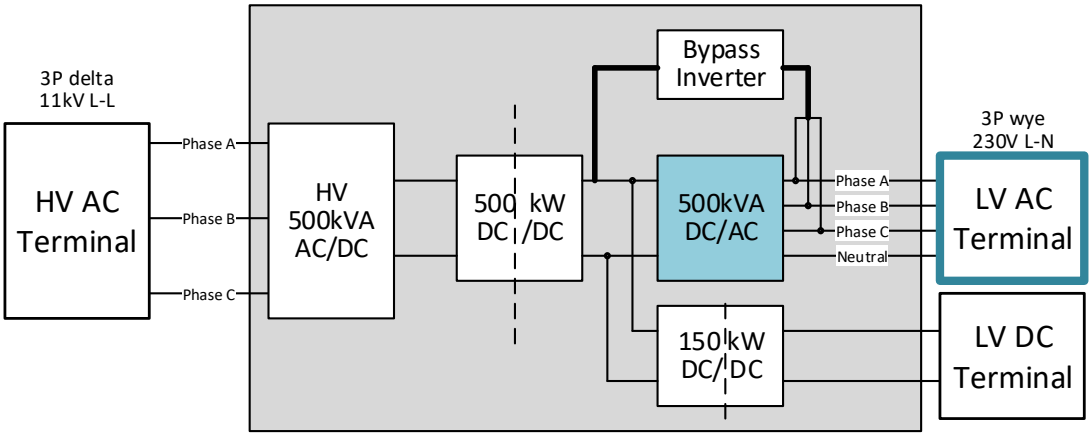


Figure 35 HV-SST 500kVA DC/AC Inverter feeds the LV-AC Terminal

5.1 500kVA DC/AC Inverter for SST Topology 2

The purpose of the 500kVA DC/AC inverter is to transform the internal DC bus voltage into a phase-independent controlled AC source at the grid edge for the AC customers. The inverter must function in both radial and interconnected network arrangement, allow for independent (per phase) control, work in all four power quadrants, and operate under extreme imbalance load scenarios (up to 100%). The topology design must support these operation modes while the hardware design must be chosen for the expected voltage and current levels. A summary of these operating ranges is shown in Table 12 below.

Table 12 Inverter Parameters

Inverter Operating Conditions	Specification
Nominal power rating	500kVA
Nominal system frequency	50 Hz
System frequency range	47-52 Hz
Nominal voltage (RMS)	400V L-L (230V L-N)
Normal Voltage Range	85-110%
Setpoint Voltage Range	90-110%
Max Voltage	120% (390Vpk L-N)
Nominal Current	725Arms
Max Current	(130%) 942Arms
Max Unbalance at LV-AC-T	100%
Max Unbalance at HV-AC-T	3%
GND Isolation Rating	3kV RMS for 1min

5.1.1 Low Voltage AC Terminal Requirements

The functionality provided by the inverter includes:

- Individual phase voltage control in radial operation
- Individual phase current (and power) control in mesh operation
- Operate under 100% unbalanced loads (no load on phase, full load on another)
- Bi-directional real power flow
- Inductive and capacitive power flow

If due to any grid condition the thermal stress on the DC/AC inverter move beyond the designed ratings, the Inverter (and SST) must work to protect itself by current limiting, shutting down SST operation, or triggering the bypass functionality during an overload, among other protective measures. This system-level hardware is discussed in another section but the inverter/SST response for frequency, voltage, and current at the low voltage AC terminal are shown in Table 13 to Table 15.

Table 13 Overload current handling by the inverter

normal	Nominal LV-AC-T	normal	118-125%	125-130%	>130% peak	550%
500kVA 254Vrms (+10%)	500kVA 230Vrms	500kVA 196Vrms (-15%)	Normal for 30 sec, bypass	Normal for 3 sec, bypass	Current limiting until bypass	Bypass Contactor Rating
			230Vrms 590-625kVA	230Vrms 625-650kVA		
656Arms	**725Arms**	850Arms	855-906 Arms	906-942 Arms	>1332Apk	4000Arms

Table 14 Frequency handling by the inverter

Frequency	Operation
>52Hz	Enter Standby
50.5-52Hz	Alarm Triggered
50.5Hz	Normal
50Hz	Nominal
49.5Hz	Normal
47-49.5Hz	Alarm triggered
<47Hz	Enter Standby

Table 15 Voltage handling of inverter

<20%	20-85%	85%	Nominal (100%)	110%	110-120%	>120%
Immediate Standby	3 sec normal operation, then standby	Normal	Nominal	Normal	3 sec normal operation, then standby	Immediate Standby
<46Vrms	46V-196V	196	230Vrms L-N (400V L-L)	253V	253-276V	>276V (>390Vpk)

5.1.2 Neural connection, 4th Leg

The conventional transformer provides a separate neural wire connection, in the SST Topology 2 this neutral connection will be through a 4th leg within the inverter as shown in Figure 36. The inverter below is created with four legs: one for each of the three phases and neutral for the SST low voltage AC output. Each leg is pictured as a half bridge with two devices operating between the internal DC bus terminals and the midpoint driving an L/C filter output.

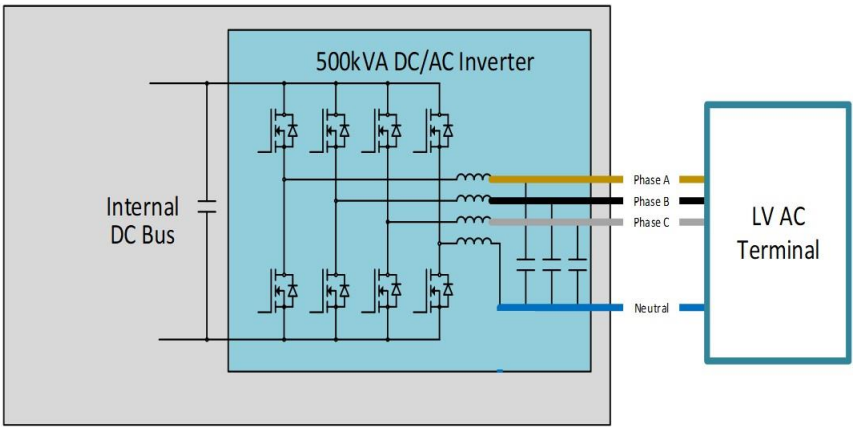


Figure 36 Leg Inverter Topology

Importantly, this 4th leg neutral also allows the independent control of output voltage (radial) and current (mesh) for each phase. As shown in Figure 37 each phase operates with its own independent half-bridge leg and is referenced to the 4th neutral leg that acts as a DC bus midpoint.

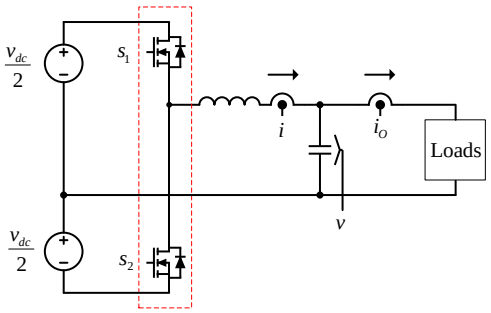


Figure 37 Model of independent phase control

5.1.3 Hardware-driven Design

With the topology in Figure 36 defined to meet the LV Engine overall functional requirements, the next challenge was to find and select hardware to meet the voltage and current requirements for the system.

Originally, EGB believed the internal DC bus voltage could be 800Vdc. This allowed us to use 1.2kV devices which are available from numerous suppliers at a wide range of current levels. However, closer inspection of the wide operation requirements for the rectifier/input stage, this inverter module, and the DC output module revealed we would need an internal bus voltage of 900-1000Vdc. Table 16 shows the internal DC bus requirements for the inverter, but the internal DC bus operating voltage impacts the design of almost every module and careful design considerations are reviewed in each section. For example, varying DC-link voltage with the AC input was discussed, but it is prudent to provide a consistent voltage to the DC/DC stage to ensure high efficiency. Instead it was decided to design around a static 950V DC bus voltage across all operation points.

Table 16 Internal DC bus requirements for inverter output

	-20%	-10%	nominal	+10%	+20%
Output AC Inverter Voltage	184V	207V	230Vrms	253V	276V
Minimum Internal DC bus voltage	578V	650V	723Vdc	795V	867V

Any bus voltage above 800Vdc does not leave enough margin for operating 1.2kV devices and therefore alternative methods for safely operating at a higher voltage should be considered. The two design concepts considered for the trade-offs and further design assessments:

1. A three-level layout with lower-voltage Silicon IGBT devices, Figure 38;
2. A two-level layout with higher-voltage Silicon Carbide MOSFET devices, Figure 39.

First, by creating three levels between the internal DC bus instead of two, the three-level layout allows the use of 1.2kV devices again. Furthermore, while Si must operate at a lower frequency than the SiC, the arrangement of the IGBT's in a 3-level design increases the effective switching frequency seen by the inductor, decreasing the magnetics requirements and effectively negating the switching frequency impact. Overall, the 3-level design is a strong contender as it combines the magnetics reduction of a SiC design with the reliability of IGBTs.

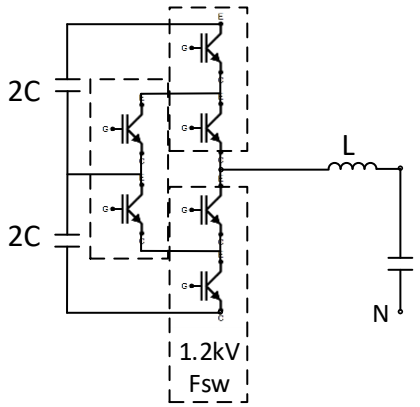


Figure 38 Three-level layout with Si IGBT

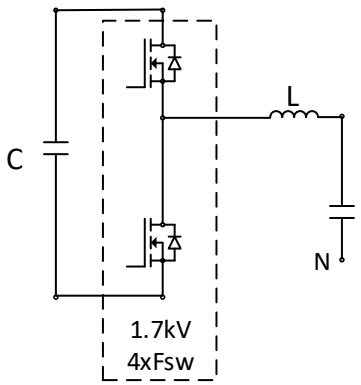


Figure 39 Two-level layout with SiC MOSFET

It was decided on the second approach. The EGB team has experience in developing two-level SiC power electronics and believe we can leverage the lessons and resources from other projects for this development. The two-level layout and MOSFET devices are also more easily paralleled to achieve higher power and/or modular flexibility. While the SiC market is ever-expanding, there are only two options available at this time for a prototype at the appropriate voltage: 1.7kV Cree/Wolfspeed CAS300M17BM2 and the 2kV Infineon FF4MR20KM1. The Infineon option was chosen for better cost, lower losses, and better design team support.

Both choices have functional current ratings around 250Arms. To achieve the desired 942Arms max current rating, as shown in Figure 40, four devices are needed in parallel for a functional current rating of 1000Arms. After several iterations, we have chosen this layout. Here, modules A&B are directly in parallel as are modules C&D; this is referred to as hard paralleling. The combinations of A&B and C&D are then paralleled after the inductor. Current sensors will be placed on each inductor so that the DSP can control balance between the inductors. A further benefit with this method is that A&B can be interleaved with C&D to reduce the switching frequency ripple currents on the output, minimizing harmonic distortion.

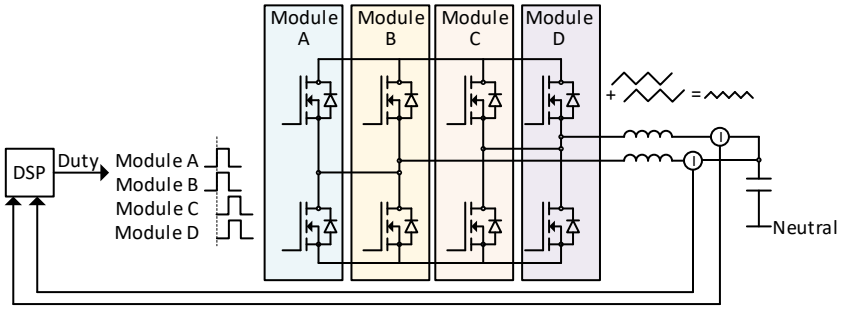


Figure 40 Parallel method for each inverter leg

This approach also reduces the stress on the output filter components: the inductors each handle half of the load current while interleaving reduces the current ripple seen by the output filter capacitors. The LC filter design is based around the switching frequency (20kHz) of the devices and the current handling requirements of the system. The design principle aims for an LC filter cut-off of less than 1/10th of the switching frequency, which translates to less than 2kHz.

The inductor manufacturer is CTM Magnetics based out of Tempe, AZ. CTM Magnetics was chosen for their experience in the design & manufacturing of liquid cooled magnetics for high power applications. EGB is working with CTM to design a 200uH inductor rated for 400A normal operation. Each inductor will form half of the paralleled phase for a total nominal current handling capability of 800A per phase, with inductance stability up to an overload of 1200Arms. The AC filter capacitor will be a 50uF TDK/Epcos capacitor with 4 in parallel for an equivalent capacitance of 200uF. The LC combination of 200uH and 200uF produces a cut-off frequency of 796Hz, which is well below 1/10th of the switching frequency.

For this design EGB have added considerable margin to ensure operation across a wide range of conditions. We have also chosen film capacitors for the AC output and have chosen to liquid cool both the inductors and silicon carbide devices – all in an effort to achieve high power density while selecting components with a long lifetime and ensuring they do not go beyond detrimental thermal limits.

5.2 500kVA AC/DC Rectifier and DC-DC Converter

The SST Topology 2 does not require a low frequency transformer in its power path. However, the replacement of this low frequency transformer by suitable and reliable power electronics requires the following technical challenges to be resolved:

1. Due to the vulnerability to overvoltage of the power semiconductor devices, proper protection methods should be taken to meet the isolation requirements. Per 60076-3, HV-SST should survive from the 75kV lightning impulse and 28kV withstand voltage.
2. The design of HV-SST should leave sufficient margin for operational overvoltage up to 19.4kV peak.
3. Due to the limited overcurrent capacity of the power semiconductor devices, to handle the LV short circuit fault and blow the downstream buses as required, the power output of the HV stage should be oversized by 100% to about 1MVA for 3 seconds.

4. High Voltage isolation should be designed for high frequency transformer and power semiconductor devices used.
5. The utilization of multi-level structure due to the availability of commercial semiconductor devices increases the number of components and control complexity. In total there are 378 additional critical components required for the HV-LV conversion alone. This does not include the additional DSPs and Control Processors required to drive the 42 Si IGBTs and 84 SiC MOSFETs required.

The high voltage to low voltage conversion is accomplished via the 500kVA AC/DC high voltage rectifier and isolated DC/DC converter. The purpose of the HV 500kVA AC/DC rectifier is to take the three-phase high-voltage input and transform it to a cascaded medium voltage dc bus. The 500kW DC/DC then interfaces with the high voltage rectifier to provide isolation and control for the internal low voltage dc bus. These stages are only required for the HV-SST.

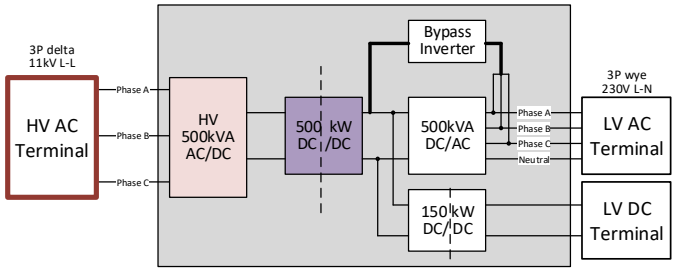


Figure 41 500kVA Rectifier and DC/DC interface with HV AC Terminal in HV-SST-A

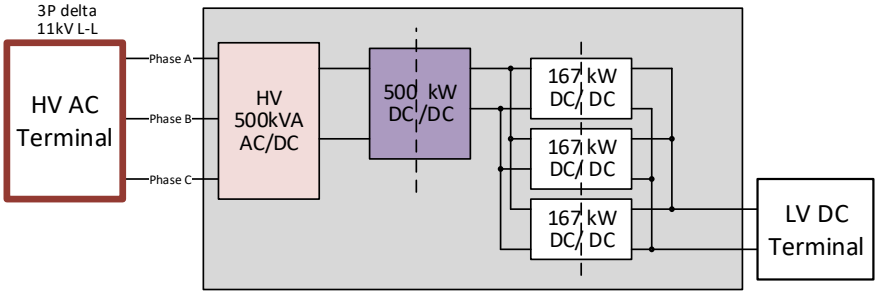


Figure 42500kVA Rectifier and DC/DC interface with HV AC Terminal in HV-SST-B

The high voltage rectifier must work in all four power quadrants, sinking/sourcing balanced reactive power as a STATCOM and providing balanced real power to/from the DC/AC and DC/DC modules via the control of the internal medium voltage DC bus. The topology design must support these operation modes while the hardware design must be chosen for the expected voltage and current levels. Due to the high input AC voltage and limited commercial availability of power semiconductor devices, multi-level topology must be applied for low voltage power devices. A summary of the rectifier operating ranges is shown in Table 17.

Table 17 HV Rectifier Parameters

HV Rectifier Operating Conditions	Spec
Nominal power rating	500kVA
Nominal system frequency	50 Hz
System frequency range	47-52 Hz
Nominal voltage (RMS)	11kV L-L
Normal Voltage Range	85-115%
Max Voltage	125% (13.7kV L-L)
Nominal Current	26Arms
Max Unbalance at HV-AC-T	3%
Applied Voltage Isolation	28kV RMS for 1min
Lightning Impulse Isolation	75kV

The isolated DC/DC converter provides a regulated internal low DC voltage and isolation as a high frequency version of the traditional transformer. To interface the low voltage inverter, 800Vdc output should be provided and power balance should be guaranteed among the multiple cascaded rectifier modules and DC/DC converter modules for better lifetime.

5.2.1 High Voltage Terminal Requirements

- Voltage step-down and isolation
- Control of the internal DC bus voltage
- Bi-directional real power control
- Reactive power control for HV-T voltage management (STATCOM)
- Maintain balanced current flowing to/from the 11kV bus

If grid conditions move beyond the designed ratings, the SST must detect the abnormal condition and protect itself by limiting the output current, shutting down SST operation, or triggering the inverter bypass functionality and other protective measures. The step-down and isolation functionality cannot be bypassed via a contactor, which handles the high fault current. Thus, both rectifier and isolated DC/DC converter must be overdesigned to provide 200% rated current. Note, the 200% capability requirement is still under SPEN EGB team assessment. The voltage, current and frequency handling capacity of the SST rectifier is shown in Table 18 to Table 21 Frequency handling by the rectifier.

Table 18 SST Rectifier Over Current Handling

normal	**Nominal HV-T**	**Normal**	**200%***
500kVA 12.6Vrms (+15%)	**500kVA 11kVrms**	500kVA 8.8Vrms (-20%)	Current limiting for fuse blowing
23Arms	**26Arms**	33Arms	52Arms

Table 19 SST Rectifier Grid Undervoltage Handling

<60%	60-80%	80-90%	90%	Nominal (100%)
standby ASAP	3sec normal operation; then standby	Normal (Alarm)	Normal	Nominal
<6.6kV	6.6kV-8.8kV	8.8kV-9.9kV	9.9kV	11kVrms

Table 20 SST Rectifier Grid Overvoltage Handling

Nominal (100%)	110%	110-115%	115-120%	120-125%	>125%
Nominal	Normal	Normal (Alarm)	3 second normal operation; then standby	3 second permissive operation; then standby	Mechanical disconnect ASAP
11kVrms	12.1kV	12.1kV-12.6kV	12.6kV-13.2kV	13.2kV-13.7kV	>13.7kV >19.4kV pk

Table 21 Frequency handling by the rectifier

Frequency	Operation
>52Hz	Enter Standby
50.5-52Hz	Alarm Triggered
50.5Hz	Normal
50Hz	Nominal
49.5Hz	Normal
47-49.5Hz	Alarm triggered
<47Hz	Enter Standby

5.2.2 Topology Options

There are several challenges in developing the SST Topology 1 rectifier stage and isolated DC/DC stage. There are ongoing works by EGB on strengthening university research relationships having a background in SST research to further better simulate and investigate the topology and hardware options for the SST input power stages. As part of this, several options have been explored to narrow the focus, highlight any challenges, and underscore requirements above, current research study and previous experiences of EGB team, SST topology is currently considered shown in Figure 43 to better define the research scope.

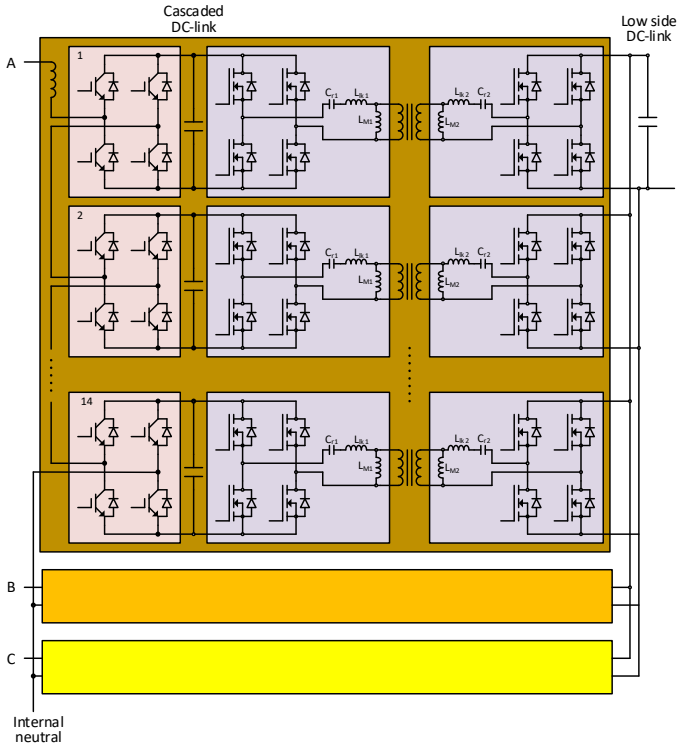


Figure 43 Input Rectifier and DC/DC Stage Possible Topology – 42 Stages Required

AC/DC rectifier

The AC/DC rectifier is composed of cascaded H-bridges to enable the circuit to handle the phase to internal neutral of 6.35kV (11kV/1.732) input using lower-voltage commercially available semiconductors. Cascaded multilevel converter has advantages over other multilevel topologies in terms of modularization, extendibility, and minimization of power semiconductors. It could provide bidirectional power flow with STATCOM capability, reduce harmonic distortion on the AC side and provide accurate regulation for DC link. IGBTs are proposed here for low cost and reliability. Each cascaded module will be interleaved to increase the equivalent switching frequency; helping to reduce ripple and audible noise. A unique design challenge of the AC/DC rectifier is that the semiconductor switches need to have HV isolation to the case while still allowing for thermal transfer to cool the switches.

The number of cascaded H-bridge stages is determined by the operational voltage. For operational voltage up to 125% of rated 11kV, phase to internal neutral voltage is up to 11.2kV. To limit the voltage across each 1.2kV IGBT to be 800V for sufficient safety margin, 14 cascaded H-bridge stages are required.

SST rectifier is used to regulate the internal medium voltage DC link, provide balanced active power control, and perform STATCOM operation by injecting balanced reactive power to the 11kV AC bus. To implement the required functions and protection from abnormal grid events, HV input voltage sensors, input inductor current sensors, and low voltage DC link voltage sensors are placed for the purpose of control. Cascaded DC link bus voltage sensors are placed for protection from cascaded DC capacitor voltage imbalance.

DC capacitor voltage imbalance is an inherent problem for multilevel converter topologies, which results from the mismatch of active and passive components, different switching patterns, limited control resolution, and different load conditions. The imbalance of the DC capacitor voltage will lead to the degradation of input current, imbalance of loss in each H-bridge, and potentially the collapse of the entire system (over voltage, over current, etc.). Specifically, 14 isolated DC/DC converters, which act as active loads, are connected to 14 cascaded DC ports to share the total power of the system. With

the parameter mismatch in the DC/DC, the power will become unequally distributed and DC voltages will diverge if no voltage balance circuit or control is properly adopted. Under this situation, some devices in rectifier stage face the risk of over-voltage failure, which may collapse the whole SST system. In the proposed topology, cascaded DC link voltage balance is implemented passively by the proposed open-loop CLLC converter. All CLLC converters are operating at fixed gain. With paralleled low voltage DC output, the fixed gain will force the capacitors at the cascaded DC link to a fixed balanced voltage.

It should be noted that there are most certainly complexity, reliability and cost trade-offs to consider when considering a 14 stage (per phase) cascaded topology of this nature that meets the design requirements and delivery of core functionalities specified in LV Engine.

For proposed cascaded H-bridge rectifier, each H-bridge module shares 454Vrms (11kV/1.732/14) and rectifies to 800Vdc.

HV isolated DC/DC

The HV isolated DC/DC stage is interfaced to the cascaded DC link and 14 stages of which are paralleled at the LV DC link. The HV isolated DC/DC has special design challenges due to the following requirements:

- It is the source of HV isolation between the HV primary and LV secondary
- Needs to be bidirectional
- Dictates voltage balance in the cascaded DC-link capacitors and power balance through the parallel modules
- Requires HV isolation between the semiconductors and case while still allowing for semiconductor cooling

Two possible topologies have been discussed for the HV isolated DC/DC – a phase shift DAB and CLLC. It is envisioned to build hardware that can support both topologies but begin by using the CLLC converter. CLLC is viewed by EGB as the preferred option due to wider knowledge base in industry and more predictable results, internal familiarity when using resonant converters in SST applications and the capability to use open loop control, simplifying implementation. The comparison chart between DAB and CLLC is shown below in Table 22.

Table 22 SST DC-DC topology options

	CLLC	DAB
ZVS	Full load range ZVS	No ZVS at light load
Bidirectional power flow capability	Yes	Yes
Open loop	Yes	No
Closed loop	Yes	Yes
Short circuit protectable	No	Yes

Bidirectional full-bridge CLLC resonant converter, which has a symmetric LLC resonant network, can operate under high power conversion efficiency with zero-voltage switching capability for primary power switches and soft commutation capability for output rectifiers. Besides, it does not require snubber circuits to reduce the voltage stress of the switching devices because the switch voltage of the primary and secondary power stage is confined by the input and output voltage, respectively. Open loop operation is another advantage over dual active bridge converter, which simplifies the control and reduces the number of sensors. Due to the features of open-loop operation, no sensors are required for control. Cascaded DC link bus voltage sensors are placed for protection, which are shared with SST Topology 2 rectifier stage. The lack of inherent short circuit handling capability in CLLC converter, will be protected via both hardware & software protection. Once the LV DC link voltage is below 480V (60% of 800V), or the DC current is beyond 200% of rated current, the system will be instantly shut down.

For proposed CLLC converter, the resonant frequency is designed to be 30kHz to reach 1:1 voltage gain. Both input and output voltage are regulated to 800V. 1.2kV SiC MOSFETs are applied in the proposed CLLC converter.

5.2.3 Hardware Selection

In this section, critical components of the cascaded AC/DC converter and isolated CLLC converter are selected and summarised in Table 23.

Table 23 SST Critical Component

Device	Stage	Function	Main Specs	Part Number (Initial design)	Supplier	# Per Stage	Total #
Si IGBT	CHB	Main Power Device	1200V, 150A	F4-150R12KS4	Infineon	1	42 (14x3)
Input Inductor	CHB	Reduce Current Ripple	800µH, 150A	Customized	TBD	1	42 (14x3)
DC Capacitor	CHB	Filter 100Hz Voltage Ripple	1000V, 820µF	947C471K102CDMS	Cornell Dubilier Elect.	1	42 (14x3)
SiC MOSFET	CLLC	Main Power Device	1200V, 50A	F4-23MR12W1M1P_B11	Infineon	2	84 (28x3)
DC Capacitor	CLLC	Filter High frequency Ripple	15A at 30kHz, 1kV, ESR<0.3Ω	947C471K102CDMS	Cornell Dubilier Elect.	1	42 (14x3)
High Frequency Transformer	CLLC	High Voltage Insulation	30kHz, 1:1, 25kW	Customized	TBD	1	42 (14x3)
Resonant Inductor	CLLC	Resonant Tank	44µH at 30kHz, 40A	Customized		2	84 (28x3)

The fundamental block of the H-bridge rectifier is shown in Figure 44. Si IGBT, input inductor and DC capacitor are required to be specified.

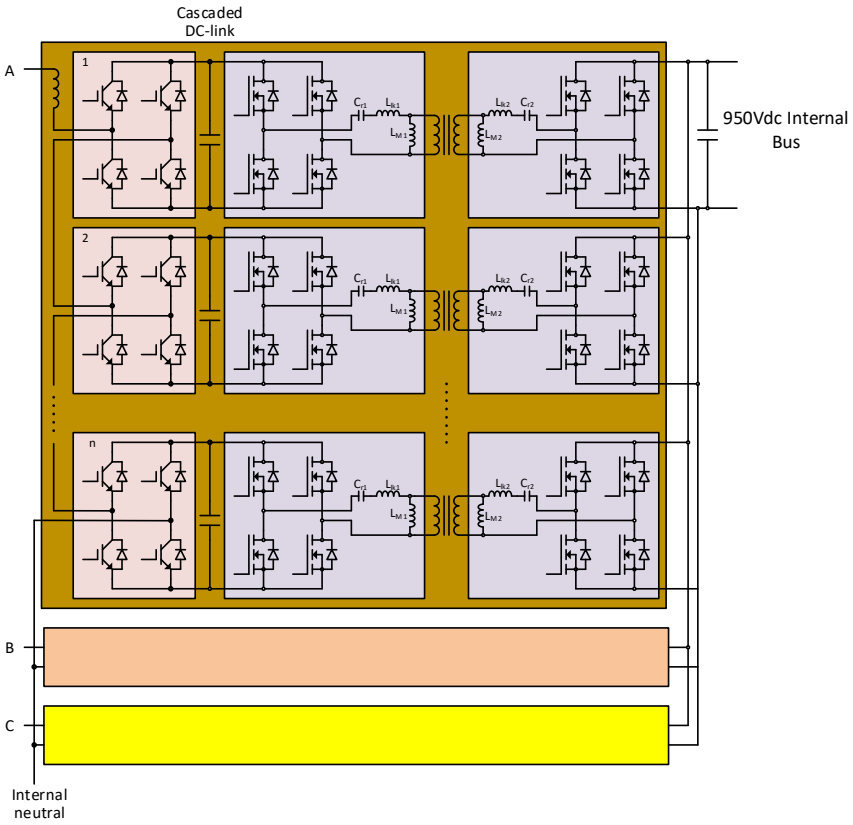


Figure 44 Fundamental block of H-bridge

Si IGBT:

As shown in Figure 44, for each phase, 14 stages of H-bridge rectifier are applied, which requires 14*4 = 56 of 1.2kV IGBTs, and 56*3 = 168 of 1.2kV IGBTs in total. Si IGBT are applied for low cost and high reliability but have an efficiency trade-off. Dual IGBT modules or full bridge IGBT modules for 1.2kV are commercially available. Rated current for 500kVA is 26Arms at 11kV. For 2pu current capacity and 50% headroom, 150A power device is selected.

Input inductor:

The saturation current for the input inductor should be the same as the power device, i.e. 150A.

The required inductance can be calculated as:

$$L \geq V_{hacm}\left[\frac{V_{hdc}-V_{hacm}}{f_{eq}I_{rpp}V_{hdc}}\right] = 1.1\text{mH}$$

Where, V_{hdc} is the total high voltage DC bus voltage (800*14=11.2kV), V_{hacm} is the maximum value of input AC voltage (8982V), and f_{eq} is the switching frequency (5k*14=70kHz). I_{rpp} is the ripple current, which is designed to be 15% of peak-to-peak value of the rated input current. For the HV-SST cascaded H-bridge rectifier, 14 distributed inductors are used rather than one centralized one, each of which is $800\mu\text{H}$.

DC Capacitor:

The DC capacitor is to suppress the double-line frequency ripple voltage. The DC capacitance can be calculated as:

$$C_h = \frac{I_{hac}}{2f_{ripple}\left(\frac{V_{hdc}}{14}\right)\cdot 20\%} = 820uF$$

Where I_{hac} is the rms value of the input current (26A), f_{ripple} is the 100Hz double line frequency. 14 film capacitors with 1.2kV or above voltage rating are placed at the cascaded DC link.

Isolated DC/DC converter

The topology of the CLLC converter is shown in Figure 45. SiC MOSFET, resonant inductors and capacitors are required to be specified.

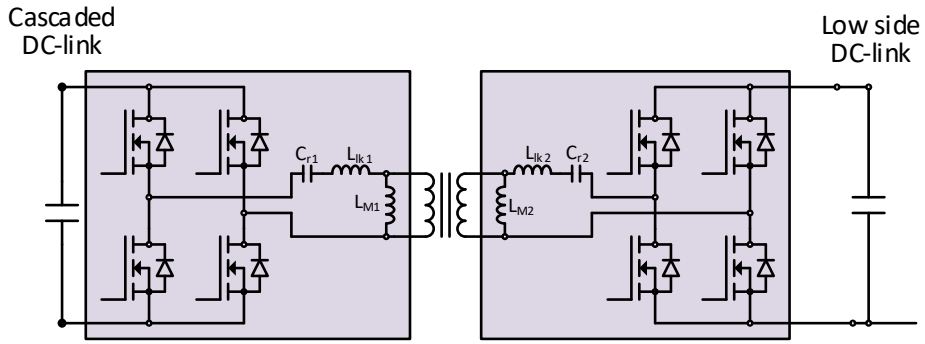


Figure 45 CLLC Converter Topology

SiC MOSFET:

For 2pu current capacity, 25kW/800 = 31.25A. So 1.2kV 50A SiC MOSFET is used in the CLLC converter.

High Frequency Transformer:

The isolated DC/DC converter will be open-loop operating at 30kHz for unity gain. Consider the 2pu current capacity, 25kW power rating transformer is selected. Turns ratio should be 1:1, and the nominal voltage for input and output is 800V.

Resonant Components:

$$R_{ac\_min} = \frac{8}{\pi^2} \cdot \left(\frac{N_p}{N_s}\right)^2 \cdot \frac{V_{out}^2}{P_{o,max}} = 20.75$$

$$Q_{max} = 0.4 = \frac{\sqrt{L_r/C_r}}{R_{ac\_min}}$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} = 30kHz$$

$$m = \frac{L_r + L_m}{L_r} = 6$$

$$L_r = 44\mu H, L_m = 220\mu H, C_r = 0.64\mu F$$

5.2.4 Start-up and Protection

5.2.4.1 Soft Start-up process

A soft start-up process is required for high voltage rectifier, in which huge inrush current may damage the power semiconductor devices. Figure 46 shows the typical DC bus voltage of a rectifier using a soft start algorithm. The system is first charged through a resistor connected between 11kV bus and the cascaded H-bridges in order to avoid a large inrush current. The resistor is then bypassed, and a diode charge is performed to charge the DC capacitor voltage. When the diode charge is finished, a ramp current charge with only the current loop regulation is used to further charge the DC capacitor voltage and approach the rated value. Finally, the DC outer loop is closed to perform the steady state regulation.

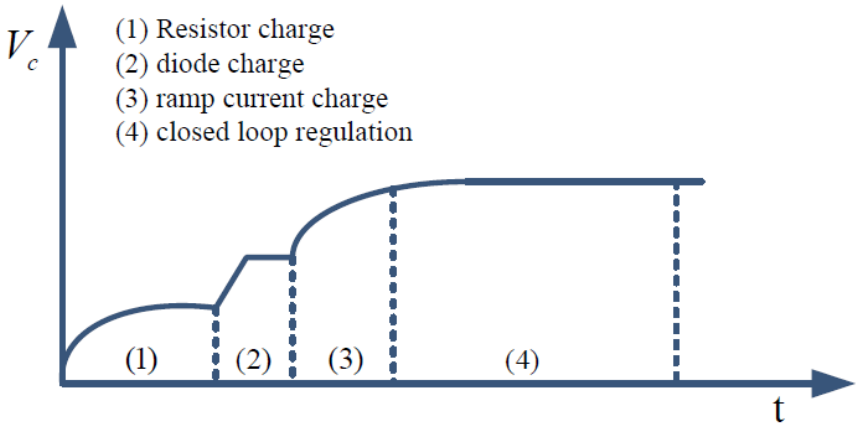


Figure 46 Soft-Start algorithm of rectifier

5.2.4.2 System Protection

Overvoltage Protection & Undervoltage Protection - As shown in Table 18 to Table 20, SST detects the HV grid voltage and goes into standby instantly when grid voltage is beyond 125% or below 60% of rated voltage.

Overvoltage Protection & Undervoltage Protection - For overcurrent, short-term overloading and instant fault protection are provided:

- Short-term overloading - HV-SST could provide up to 130% rated current for 30 seconds before current limiting to 100% rated current.
- Instant-fault protection - SST limits the current at 200% rated current for 3 seconds to allow the LV downstream fuses to clear before SST stops (switches off) operation when short circuit occurs at the LV terminal. Further verification is required with power system simulation.

Frequency Protection - Grid frequency is monitored by SST. Once abnormal frequency is detected, SST switches into standby instantly.

Internal Fault Protection - Other than the system protection, internal protection is required to protect the power stage of the SST:

- Cascaded dc link voltage imbalance protection - Although balanced cascaded DC link voltage could be implemented by the open-loop operation of the CLLC converter, voltage imbalance will be monitored, if voltage deviation is beyond 20V, SST should go into standby.
- Over temperature protection - Temperature sensors are placed at hotspots of the critical components. Once temperature is detected high, SST should warn and go into standby as required.

5.2.5 System Isolation/Insulation Requirements

The insolation requirements for the SST are in the bottom row, most notably 28kV RMS withstand and 75kV Peak Lightning impulse.

2.20 Insulation requirements

The insulation requirements of **SST** shall comply with IEC 60076-3, IEC 62477-1, and IEC 62477-2 where applicable. Table 6 shows the insulation requirements for conventional transformers as specified IEC 60076-3.

Table 6 – Insulation requirements for conventional transformers

Highest voltage for equipment (kV r.m.s)	**Nominal voltage** (kV)	**Rated lightning impulse voltage** (LI) (kV Peak)	**50 Hz withstand voltage** (kV r.m.s)
1.1	0.40/0.23	-	3.0
7.2	6.6	60.0	20.0
12.0	11.0	75.0	28.0

The **SST Manufacturing Partner** shall be responsible for carrying out all the insulation coordination studies according to IEC 60071 and providing results to SPEN.

All the internal clearances between phases, phase- earth and phase to neutral at the terminations and between them shall comply with IEC 62477.

5.2.6 HV-SST Enclosure dimensions (estimated)

This initial estimate is based primarily on the Critical Component Table 23 additional heat load of the individual components, the high voltage isolation/insulation requirements, and lightning requirements of IEC 60076-3 as the key factors. This 42-stage HV-SST will add approximately 2.0 cubic meters of overall volume to the last stage DC/AC last stage of 1.5 cubic meters. At early stage of the project, when EGB team started the development of SST Topology 1, the back to back (AC/DC/AC) arrangement was considered. The “reduced size” SST Topology 1 target began initial conceptual work released and then it was terminated in preference to the much lower complexity & size topology explained in Section 4.

5.3 Isolated DC-DC Output (500kW and 150kW)

The purpose of the 150kW and 500kW DC/DC modules is to take the internal DC bus, add isolation, and control the output power and voltage for grid-level DC services such as lighting, EV charging, and distributed energy. Both the SST Topologies contain this module, as shown in the highlighted image below. The SST has both a type-a and type-b version requiring 150kW and 500kW, respectively. For hardware simplicity a single 167kW capable DC/DC module is designed such that when three are stacked together 500kW capable hardware is achieved. When design requirements are discussed, the 150kW and 500kW will be the foundation; when hardware is discussed, this 167kW power level will be invoked.

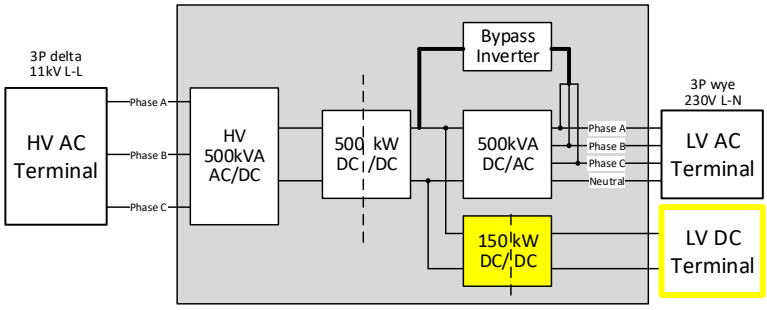


Figure 47 HV-SST-A 150kW (167kW) DC/DC stage feeds the LV DC Terminal

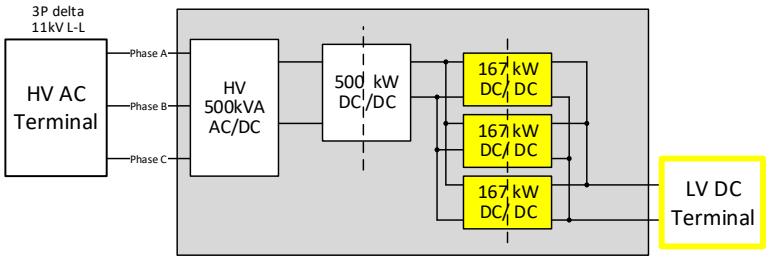


Figure 48 HV-SST-B 500kW DC/DC stage is made up of three 167kW stages stacked in parallel and feeds the LV DC Terminal

The DC/DC must offer seamless transition for bidirectional power flow, isolation, short circuit protection, and efficient operation across the load range. The topology design must support these operation requirements while the hardware design must be chosen for the expected voltage and current levels. A summary of the operation requirements is shown in the table below.

Table 24 0-1 DC/DC Parameters

DC Operating Conditions	150kW Spec	500kW Spec
Nominal power rating	150kW	500kW
Nominal output voltage	950Vdc	950Vdc
Nominal load current	158Adc	526Adc
Max output voltage ripple	±20V	±20V
Max load voltage	1000V	1000V
Max load current	167A	556A

5.3.1 DC Terminal Requirements

The DC terminal may be connected to a variety of "new" DC grid-edge loads including lighting, EV charging, office buildings, and distributed energy. The DC terminal will control a fixed 950Vdc output voltage. This new DC micro-grid requires different overload handling than at the AC terminals: most notably, it is expected that the loads will mostly be other power-invariant power electronics. Thus, traditional overload-reducing methods such as drooping voltage will no longer decrease power demand. As a result, the DC terminal overload operation range does not focus on voltage and current separately, but on different power operation modes.

Table 25 Overload Protection of 500kW DC/DC Module

Operation Mode	Immediate Standby	Current Limiting	Power Limiting	Nominal	Power Limiting	Immediate Standby
Power		472-500kW	**500kW**	500kW	**500kW**	
Voltage	<850Vdc	850-900Vdc	900-950Vdc	**950Vdc**	950-1000Vdc	>1000Vdc
Current		**556Adc**	526-556Adc	526Adc	500-526Adc	

Table 26 Overload Protection of 150kW DC/DC Module

Operation Mode	Immediate Standby	Current Limiting	Power Limiting	Nominal	Power Limiting	Immediate Standby
Power		142-150kW	**150kW**	150kW	**150kW**	
Voltage	<850Vdc	850-900Vdc	900-950Vdc	**950Vdc**	950-1000Vdc	>1000Vdc
Current		**167Adc**	158-167Adc	158Adc	150-158Adc	

5.3.2 Isolated topology

Various DC/DC topologies have been considered against the hard requirements, including:

- Bidirectionality with seamless transition between positive and negative power flow
- 850-1000V output voltage regulation between no load to full load
- Protection against short circuit events
- Isolation between input and output

Table 27 Topology options for DC/DC Converter

Criteria	DAB	CLLC	CLLC+buck	3-level
Bidirectionality (seamless transition)	✓	✓	✓	✓
850-1000V output regulation	✓		✓	✓
Protection against short circuit	✓		✓	✓
Isolation	✓	✓	✓	

Initially a 3-level flying capacitor topology was proposed for LV Engine. This solution allowed for the use of 1200V devices to operate a DC output of over 900V and meets 3 out of 4 of the requirements. However, the lack of isolation means the internal DC-link could accidentally be grounded by a customer, impacting inverter operation. Other options such as the CLLC could not handle short-circuit limiting and the CLLC + Buck becomes a two-stage design which increases component count and decreases efficiency.

Thus, EGB settled on a Dual Active Bridge (DAB) topology, as shown in Figure 49. The principle of operation for a DAB is analogous to the leading/lagging power factor concept in an AC system. The primary and secondary full bridges of the DAB each create a fixed high frequency square wave. Next, power flow through the DAB is controlled by shifting the phase between the primary and secondary, just as an inductive and capacitive load create a lagging and leading current in an AC system, respectively. In a short circuit event, the DAB will set the phase shift to 0 to cut power flow. To transition from positive to negative power flow the controller simply adjusts from a positive to negative phase shift angle for a seamless transition.

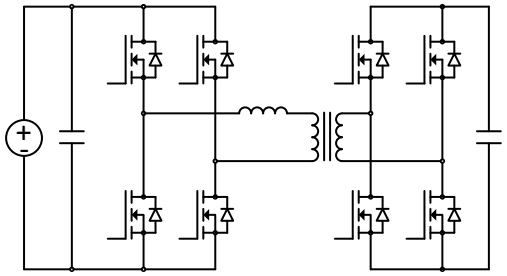


Figure 49 Dual Active Bridge (DAB) topology

5.3.3 ZVS, Burst Mode, and Overload Operation

One challenge with designing the DAB involves ensuring operation in zero voltage switching (ZVS) mode, also referred to as soft switching, to avoid high device losses and possible failure. As shown in Figure 50 below, there exists a careful balancing act between leakage inductance, voltage gain, and output power. Larger leakage inductance results in a wider ZVS range throughout the output power range, but also creates higher RMS currents which results in higher conduction losses.

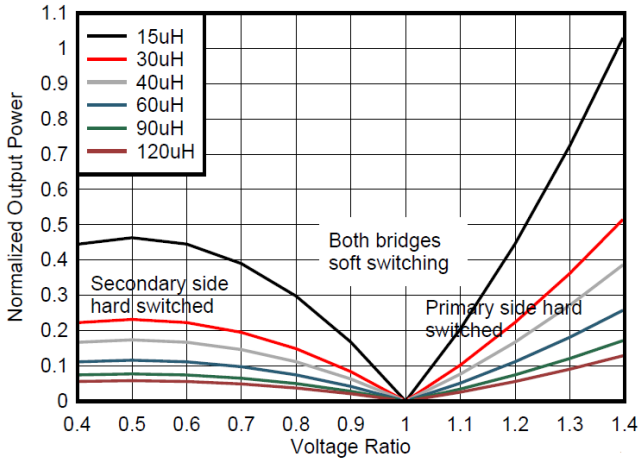


Figure 50 ZVS region

Light load conditions are detrimental to achieving ZVS. To deal with this issue, EGB proposes to operate the DAB in burst mode. Bust mode means in a light load condition the DAB will operate in two states: (1) on with enough phase shift to achieve at least partial ZVS and (2) completely off. This is a common approach for DC converters to maintain output voltage with minimized losses. Thus, without human/SPEN interaction, the DC service can optimize its efficiency under no-load conditions (when no electric vehicles are charging or during daylight hours when street lights are not needed). When a load is sensed at the terminals, normal operation is seamlessly resumed.

A single internal DC bus voltage helps simplify this ZVS operating range and the DC/DC design. Thus, while the AC terminals could have tolerated a modulated internal DC bus based on the input and output voltage requirements, the DC-DC stage operates more predictably with a fixed, known internal DC bus voltage. Furthermore, the selection of 950Vdc for both the internal DC bus and external voltage terminal helps meet both the input and output AC terminal requirements while simplifying the ratio requirements of the DC/DC isolation transformer.

5.3.4 Hardware Based Design

The most important design elements are the selection of the leakage inductor, desired phase shift of operation, output capacitor rating, switching frequency of operation, selection of SiC MOSFETs, transformer, and intended ZVS range of operation. Many of these design parameters are interrelated, and selection of any one of them has a direct impact on the others. For example, the selection of leakage inductor has a direct effect on the maximum power transferred, which in turn affects the phase shift of operation of the converter at the intended power level.

A 9uH leakage inductance is selected and will be integrated into the transformer design. This critical value may be adjusted as required by further testing. By increasing the inductance, the ability for soft switching of the converter extends down to a very low power level (light loads), leading to better switching performance with less switching losses. Yet, increasing the leakage inductance leads to increased RMS currents in the primary and secondary of the transformer and ripple currents in the capacitor, resulting in more conduction losses.

The magnetizing inductance is chosen to be generally ten times the value of leakage inductance as a starting point for optimization. While the leakage inductor is important for providing soft switching up to 1/2 or 1/3 of the rated load, the magnetizing inductance of the isolation transformation then takes over ensuring soft switching near light loads. EGB has teamed up with Murata to develop both a high-frequency and high-power transformer to meet the magnetizing inductance, leakage inductance, thermal handling, and isolation requirements of this transformer.

The output ac filter capacitor of the dual-active bridge must be sized to handle the output ripple, impacting the terminal voltage specification. EGB believes that 850uF of capacitance per 167kW module should meet our EV charging partner, Tritium, input requirements. This will be composed of a variety of capacitors to meet the different frequency needs and, where appropriate, re-use AC filter and internal DC bus capacitor hardware already selected.

The SiC module selected for the inverter and low voltage rectifier stage will also be used here. SiC has several advantages for a DC/DC DAB:

- The switching speed of the SiC MOSFET is faster than a traditional Si device, thereby easily meeting the audio DB requirements and reducing the size of passive magnetic components, increasing the power density;
- The reverse recovery charge is significantly smaller in the SiC MOSFET for DAB application, resulting in reduced voltage and current overshoot;
- Lower state resistance will significantly reduce conduction losses;
- The switches have the ability to block higher voltages without breaking down.

All components of the DC/DC module are sized with adequate margin and film capacitors are selected to optimize lifespan across the full operation range.

5.3.5 DC/DC Control and Operation

The SST will offer SPEN unprecedented vision and control into the grid-edge of their network. The low voltage DC output stage will capture and report the following real time grid values:

- LV DC Secondary Terminal Voltage
- LV DC Secondary Terminal Current
- Real Power (kW) magnitude and direction at the LV DC Secondary Terminal

Figure 51 shows the power module, interface sensor card, and control module (SiCSM) interact with each other for the bidirectional energy transferring between 950V DC Link from the Rectifier and the isolated 950V DC output. These three components will provide isolated sensing, calculations for closed loop control, and power handling.

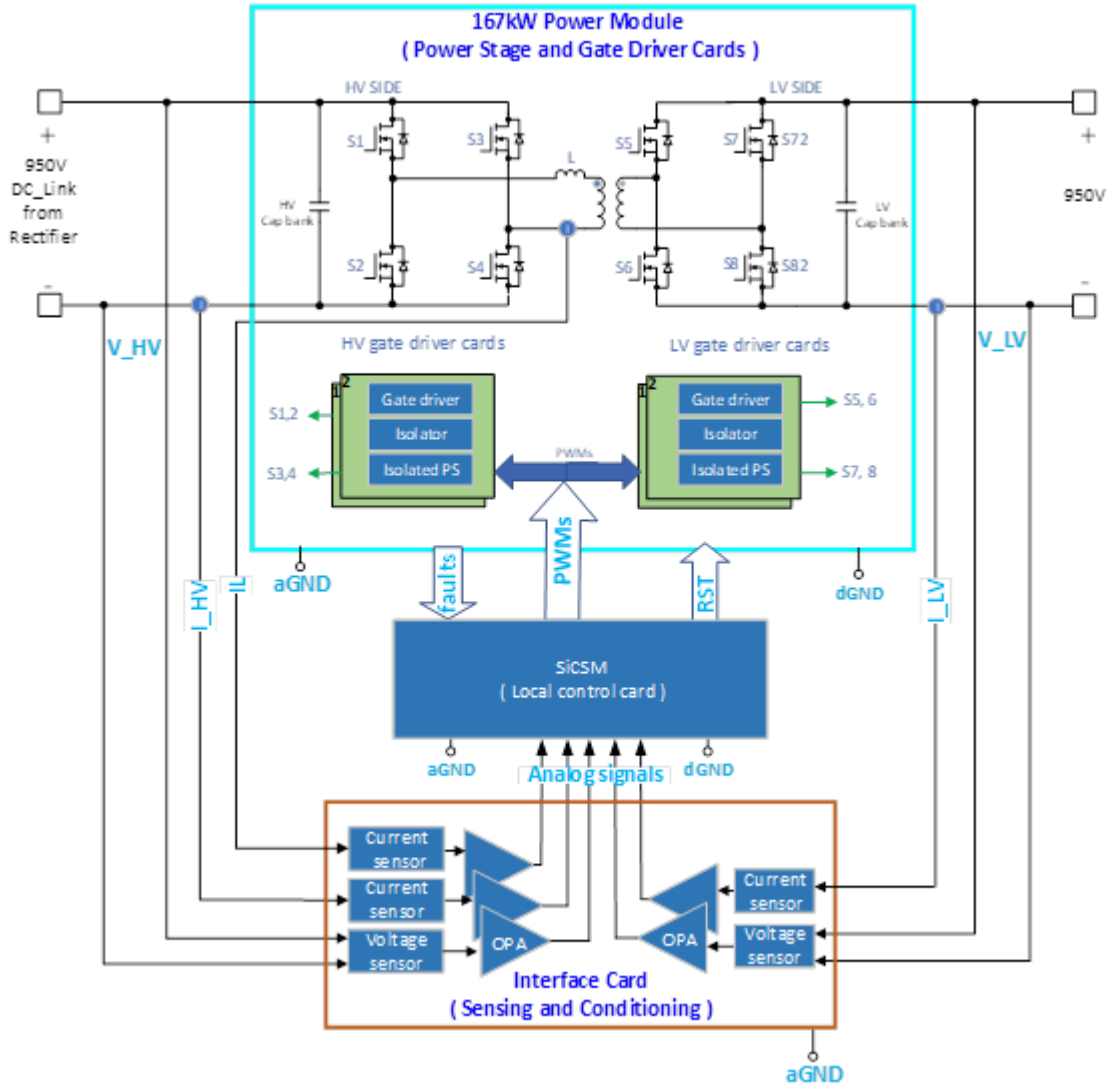


Figure 51 Complete 150kW DC Service Sub-Assembly

5.4 Academic and Industry Engagement

To accelerate progress and break ground on the toughest challenges, specifically the HV to Isolated DC conversion, EGB agreed to add additional qualified resources and/or key technology to the SPEN SST Topology 2 development program. EGB pursued noted power electronics programs at four universities where existing relationships exist:

5. University of Texas, Austin: Semiconductor Power Electronics Center (SPEC) – Dr. Alex Q. Huang (SPEC Director)
6. North Carolina State University: NSF FREEDM Systems Center – Dr. Iqbal Hussain (FREEDM Director)
7. Virginia Tech: Future Energy Electronics Center (FEEC) – Dr. Jason Lai (FEEC Director)
8. University of Colorado, Boulder: Colorado Power Electronics Center (CoPEC) – Dr. Dragan Maksimovic

EGB evaluated the technology developments at SPEC (UT-A), FREEDM (NCSU) and FEEC (VT) for possible commercial advancement for use in the LV Engine application. After evaluation and additional research, the detailed technology advancement focused on UT-A revealed an Unfolding Bridge & DAB topology using an experimental "SuperMOS" Cascode 7.2kV SiC module and

experimental HV DAB Transformer1. This solution is currently an early single-phase lab prototype and after series of deep technical evaluation, risks/rewards assessment and due diligence EGB concluded that the UT-A prototype cannot be deployed in LV Engine development.

- Unfolding Bridge & DAB topology offers no simplification or de-risking for LV Engine 4-quadrant requirements and may be additional risks may be introduced. This topology was chosen by UT-A as an enabler for the SuperMOS Cascode SiC module implementation.

- SuperMOS Cascode 7.2kV SiC initially looked promising, specifically the isolated power supply. But more Q/A revealed too much risk of a non-commercial SiC device. Unproven areas:
  - Possible false triggering due to noise (no negative turn-off voltage)
  - Not in-circuit tested (active converter) above 2.4kV, designed for 7.2kV
  - Balancing across 6 x 1.2kV internal cascaded devices
  - Voltage Isolation risk with experimental packaging
  - 11kV requires cascading three 7.2kV modules to meet the voltage requirement
- HV Transformer. This is the best part of their proposal, but EGB feel we can get a superior commercially built part that will prove more reliable in this high voltage stress environment.

- Both the unfolding bridge topology and SuperMOS have not been applied, tested and validated in a similar 3-phase system setup, it requires substantial support from EGB for mechanical, thermal, control HW & algorithms, and fault protection during and after the planned 6 months delivery time.

EGB has also re-engaged Mitsubishi, Infineon & Wolfspeed for an update on their commercially available Si and SiC switching devices based on lessons learnt relating to topology, partitioning, modularity, reducing risk, best industry practice & commercial availability of the required supporting circuits (gate drive, power supplies, sensors). The main output of these engagements was to learn that 2.0kV SiC devices will be commercially available in Q2 2021 by Infineon with early access in Q1 2021. This can significantly reduce overall SST Topology 2 cost, improve reliability, reduce cooling requirements and size of the product developed for LV Engine.

6. Lessons Learnt and Next Step

6.1 Next Step

6.1.1 SST Topology 1

The materials and component of the SST Topology 1 have now been completely ordered and they are expected to be delivered within late Q4 2020 and early Q1 2021. According to the design and manufacturing plan, prototyping and benchtop testing are the main activities will start in Q1 2021. Manufacturing and Factory testing will commence in Q2 2021 with design changes and product manufacturing and testing completed in Q3 2021.

6.1.2 SST Topology 2

EGB is currently validating the power and thermal simulation of the Infineon 2.0kV SiC modules. In anticipation of successful power & thermal simulation results with the 2.0kV SiC modules, EGB has agreed with Infineon to reserve parts for early benchtop prototype work in Q1 2021, ordering materials in Q2, the prototyping and manufacturing are scheduled in Q3 2021.

[1] https://repository.lib.ncsu.edu/bitstream/handle/1840.20/34943/etd.pdf?sequence=1&isAllowed=y

6.2 Key Lessons Learnt

The detail design of SST topologies and components considered are provided in this report. Although each section of this report provides specific learning about the LV Engine products, a summary of key learnings is listed below:

- The UPFC design is preferable over the back to back (AC/DC/AC) design for SST Topology 1 solution. As the UPFC design offers a more efficient, smaller footprint, more reliable and less expensive solution than the back to back design. In addition, UPFC does not limit the fault current to the LV network whereas back to back arrangement does have this limitation;

- The status of LV network (radial or interconnected) may not be available to SST in a real-time basis, therefore the control strategy for delivery of SST services (e.g. voltage control or power flow control) should not rely on the real-time information from network;

- The voltage at SST LV terminal should remain stable in the event of sudden change in demand to ensure the quality of supply to the customers is not affected. For that reason, SST control strategy in response to active (P) and reactive power (Q) setpoints is to revert to voltage control mode after achieving the setpoint. In another words, SST will not lock to the P&Q set points after achieving them but will lock to the resultant voltage after achieving P&Q set points;

- The services expected from SST (e.g. voltage control, imbalance cancelation, power factor correction etc) at full rating may not be required at the same time. Designing SST for provision of all services concurrently at full rating leads to unnecessarily overdesigning the product. Instead, priority of services can be considered so that some of the services may gracefully degraded if SST reaches its thermal ratings;

- For devices connected to the HV network, the insulation requirements are to pass the impulse lightening voltage of 75kV and withstand voltage of 28kV in compliance with IEC 60076-3. In SST Topology 2 will have power electronic modules connected directly to the HV network. Although the bushing and insulation to the enclosure can be designed to satisfy IEC 60076-3 power electronic devices are very susceptible to excessive overvoltage condition. Therefore, some specific design considerations should be considered to protect the power electronic modules in overvoltage conditions. LV Engine's existing design is to stack up extra power electronic modules at HV to build the tolerance against 28kV however further design options to meet the 75kV lightening impulse are being assessed;

- The safety policy for working around grid connected capacitor devices should be considered for power electronic devices too. Capacitors may be used in the design of a power electronic device, for example SST requires an internal DC link which is constructed by series of capacitors. In order to avoid any capacitor charge shock to operation staff, SST should be fitted with a discharging mechanism. Also, operation staff should be able to test internal charges using multi-meters and test points available on SST local interface before conducting any work on SST (e.g. replacing the fuses).

- SST design for LV Engine will provide 24V DC supply through the local interface. This can be used for any telecommunication supply with no need for extra auxiliary supply in the substation. SST will be also able to issue 24V DC inter-tripping voltage to the ring main unit (shunt trip coil) which will be used in overall protection strategy.

- The spare parts required for SST should be available in the substation to ensure operation staff can have immediate access to spare parts in case of failure. SST designed for LV Engine has an allocated compartment for the spare parts especially 800A fuses.

- Power electronic devices may have limited capability in temporary overloading and adequate fault current contribution to allow operation of protection devices based on existing operation practices. More innovative solutions for fault identification and protection should be developed if power electronics are to be effectively deployed in both AC and DC distribution networks.

Appendix A Back to Back design for SST Topology 1

As mentioned, the initial design for SST Topology 1 was a back to back AC/DC/AC building block shown in Figure A-1. **Nonetheless, following the detailed design analysis, performance evaluation and mechanical design of SST Topology 1, it was decided to consider Unified Power Flow Controller (UPFC) architecture for SST Topology 1 as shown in Figure 7**. In order to provide full learnings of the project, different aspects of the design considered initially for the back to back arrangement are presented in this Appendix.

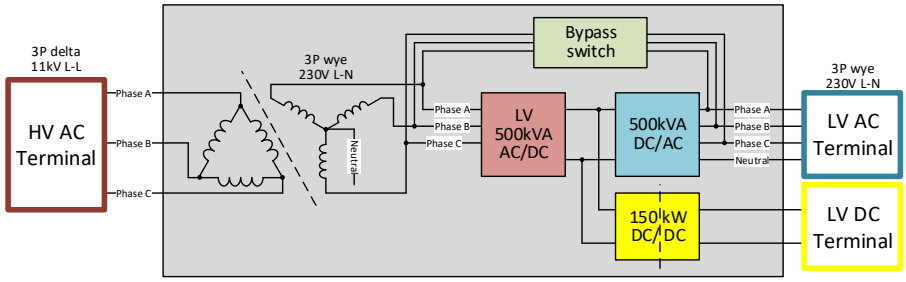


Figure A-1 SST Topology 1 initial design (AC/DC/AC) converter added to conventional transformer

A.1 500kVA AC/DC Rectifier

The purpose of the 500kVA AC/DC Rectifier is to transform the stepped-down AC from the traditional 50Hz transformer into an internal DC bus voltage, supplying real power to the low voltage AC and DC output modules and reactive power as a STATCOM for the high voltage terminal. Only the LV-SST contains this module, as shown in the highlighted image below.

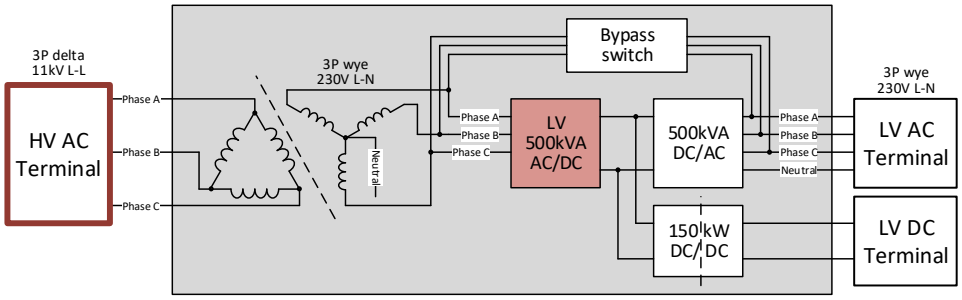


Figure A-2 LV 500kVA AC/DC Rectifier for LV-SST interacts with the HV AC Terminal

The rectifier must work in all four power quadrants, sinking/sourcing balanced reactive power as a STATCOM and providing balanced real power to/from the DC/AC and DC/DC modules via the control of the internal DC bus. The topology design must support these operation modes while the hardware design must be chosen for the expected voltage and current levels. A summary of these operating ranges is shown in Table A-1.

Table A-1 Rectifier Parameters

Rectifier Operating Conditions	Spec
Nominal power rating	500kVA
Nominal system frequency	50 Hz
System frequency range	47-52 Hz
Nominal voltage (RMS)	433V L-L (250V L-N)
Normal Voltage Range	80-115%
Max Voltage	125% (541V L-L)
Nominal Current	667Arms
Max Current	(138%) 920Arms
Max Unbalance at LV-AC-T	100%
Max Unbalance at HV-AC-T	3%
GND Isolation Rating	3kV RMS for 1min

These parameters are close enough to the requirements of the 500kVA DC/AC inverter that most hardware and components are mimicked between the two modules for the SST Topology 1.

A.1.1 LV 500kVA AC/DC Rectifier Requirements

The functionality provided by the rectifier includes:

- Control of the internal DC bus voltage
- Bi-directional real power control
- Reactive power control for HV-T voltage management (STATCOM)
- Maintain balanced current flowing to/from the transformer

If grid conditions move beyond the designed ratings, the Rectifier (and SST) must work to protect itself by current limiting, shutting down SST operation, or triggering the bypass functionality during an overload, among other protective measures. System-level hardware is discussed in another section but the rectifier/SST response for frequency, voltage, and current at the high voltage AC terminal are shown in the tables below.

Table A-2 Rectifier Over Current Handling

normal	**Nominal HV-T**	**Normal**	**+125-130%**	**130-138%**	**>138% peak**	**600%**
500kVA 288Vrms (+15%)	**500kVA 250Vrms**	500kVA 200Vrms (-20%)	Normal for 30 sec, bypass	Normal for 3 sec, bypass	Current limiting until bypass	Bypass Contactor Rating
			250 Vrms 625-650 kVA	250 Vrms 650-690 kVA		
580Arms	**667Arms**	834Arms	834-867Arms	867-920Arms	>1300 Apk	4000Arms

Table A-3 LV-SST Rectifier Grid Undervoltage Handling

	<60%	60-80%	80-90%	90%	Nominal (100%)
	standby ASAP	3sec normal operation; then standby	Normal (Alarm)	Normal	**Nominal**
Rectifier Input L-L RMS	<260V	260V-346V	346V-390V	390V	**433Vrms**
Transformer Input L-L RMS	<6.6kV	6.6kV-8.8kV	8.8kV-9.9kV	9.9kV	11kVrms

Table A-4 LV-SST Rectifier Grid Overvoltage Handling

	Nominal (100%)	110%	110-115%	115-120%	120-125%	>125%
	Nominal	Normal	Normal (Alarm)	3 second normal operation; then standby	3 second permissive operation; then standby	Mechanical disconnect ASAP
Rectifier Input L-L RMS	**433Vrms**	476V	476V-498V	498V-520V	520V-541V	>541V (765.4Vpk)
Transformer Input L-L RMS	**11kVrms**	12.1kV	12.1kV-12.6kV	12.6kV-13.2kV	13.2kV-13.7kV	>13.7kV >19.4kV pk

Table A-5 Frequency handling by the rectifier

Frequency	Operation
>52Hz	Enter Standby
50.5-52Hz	Alarm Triggered
50.5Hz	Normal
50Hz	Nominal
49.5Hz	Normal
47-49.5Hz	Alarm triggered
<47Hz	Enter Standby

A.1.2 3-Leg Topology and Component Choices

Unlike the inverter which must handle both 100% unbalanced load and maintain individual phase control, the LV-SST rectifier provides a balanced real power to the internal DC bus and sources/sinks a balanced reactive power to the secondary side of the 50Hz transformer to act as a STATCOM for the HV AC terminal.

Thus, three legs meet the control requirements, as shown in Figure A-3.

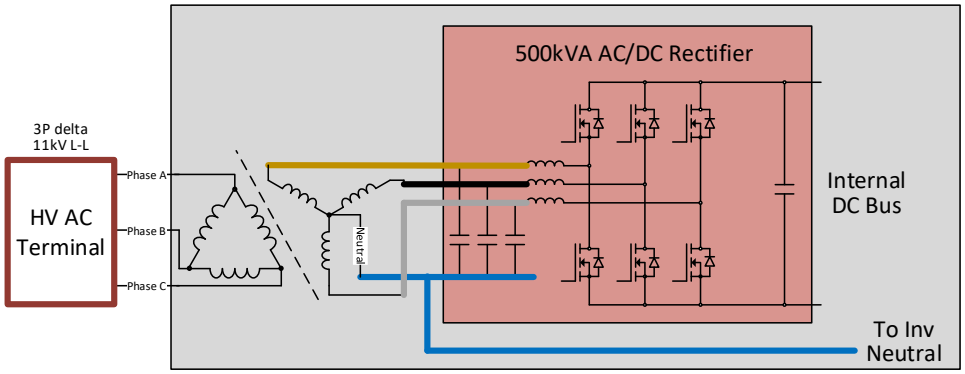


Figure A-3 LV 500kVA AC/DC Rectifier layout

The rectifier acts as a boost converter, increasing and rectifying the AC input voltage to a higher DC internal bus voltage. To ensure the control is properly boosting across the entire input voltage range, and to leave extra control margin for the STATCOM operation, a DC bus voltage of 950Vdc is selected.

Table A-6 Internal DC Bus Requirements for Rectifier

	-40%	-10%	nominal	+10%	+25%
Input AC Rectifier Voltage	184V	207V	433Vrms	476V	572V
Minimum Internal DC bus voltage (M=0.9)	408V	612V	680Vdc	748V	936V

Because of similar input/output AC voltage, current requirements, and a shared internal DC bus, the hardware of the SST Topology 1 rectifier can mirror that of the inverter. The same SiC two-level topology is chosen operating with the same SiC module, switching frequency, hard parallel and interleaving strategy for current handling, filter inductor, and AC filter capacitor. The final topology for the SST Topology 1 is shown in Figure A-4.

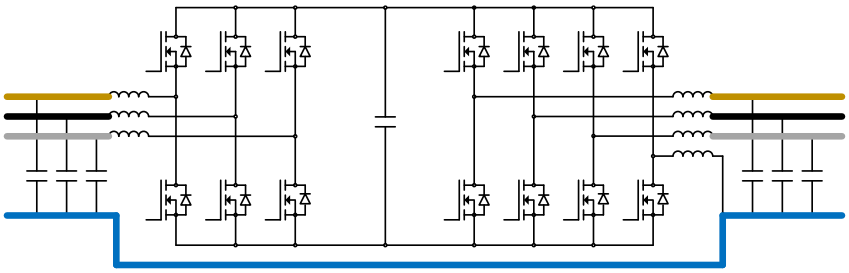


Figure A-4. LV-SST Rectifier and Inverter topology

A.1.3 Internal DC Bus Design

The internal DC bus (also referred to as DC-link) directly impacts rectifier current THD, DC output design, inverter performance, and overall system stability. While control methods will be implemented to decouple DC-link ripple from the rectifier/inverter, the hardware foundation needs to be able to support the upper limits of operation.

There will be three levels of capacitances on the DC link: bulk capacitance, SiC bypass capacitance, and snubber capacitance. All capacitors are film-type and designed with enough margin for maximizing lifespan. Each level of capacitance plays a different role. The bulk capacitance bank will be designed to handle the double-line (100Hz) frequency ripple, often caused by unbalanced loads on the inverter. After simulating 100% unbalanced loads (both real and reactive), twelve Epcos/TDK B25690C1168K503capacitors are designed in parallel for a total of 19.2mF. The resonant frequency of this capacitor, the frequency at which the capacitor is no longer effective, is 13.2kHz – so this capacitor will bypass the 100Hz current only.

Higher frequency ripples are caused by the switching frequency and the turn on/turn off speed of the silicon carbide module. The Epcos/TDK B25631B1406K500 bypass capacitor is chosen for the switching frequency and harmonics of the switching frequency. The resonant frequency of this capacitor is 145kHz. The Epcos/TDK snubber capacitor B32656S1824 will handle device level switching overshoots. These capacitors are designed specifically for 62mm packaging and will screw directly onto the + and – terminals on the SiC module, providing a low inductance bypass path.

Similarly, the DC-link bus bar capacitors need to be sized for worst case currents. Figure A-5 shows the frequency spectrum of the bus bar current with the LV-SST operating near a boundary condition. There is over 1000A of low frequency current as well as a significant amount of high frequency current, so skin effect becomes a concern. Given this information, the philosophy is to build up sufficient copper by making the bus bar wider as opposed to thicker. A wide bus bar with maximum surface area is best for both minimizing loop inductance as well as minimizing skin effect. Mersen's laminated bus bars are an ideal solution for the power stage and will likely be the bus bar manufacturer for the LV-SST. Laminated bus bars are composed of layers of interleaved copper with insulation material in between layers. Such designs maximize capacitance and minimize loop inductance which in turn minimizes unwanted ringing noise due to resonance caused by loop inductances.

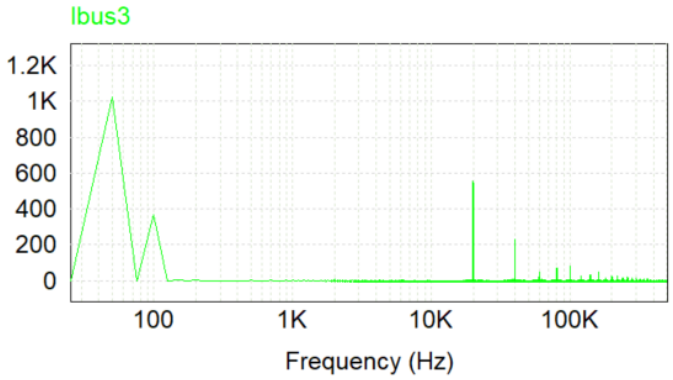


Figure A-5. Current stress on bus bar

A.1.4 Rectifier Control and Operation

The SST Topology 1 will offer unprecedented vision and control into the grid-edge of their network. The inverter stage will capture and report the following real time grid values:

- L-L RMS Voltages at the HV Primary Terminal
- RMS Current and phase angle at the HV Primary Terminal
- Real Power (kW) magnitude and direction at the HV Primary Terminal
- Reactive Power (kVAR) magnitude and direction at the HV Primary Terminal
- High Voltage Terminal Frequency
- High Voltage Terminal THD

SPEN will be able to toggle and control in real time setpoints for the following parameters:

- HV voltage deadband (STATCOM)
- Reactive power injection slope (STATCOM)

Grid Syncing

A Phase Locked Loop (PLL) will be used to sync the SST to the grid (HV Terminal) frequency at the input rectifier stage. This information will then be provided to the Inverter control in radial mode to determine the output phase angle.

When SST substation is interconnected to another substation, however, two different grids will be "meshed" together. This will require the Rectifier module to continue to operate with a PLL synced to the HV Terminal while the Inverter shifts to its own unique PLL to sync up with a grid formed by another transformer. In Mesh operation, the Inverter module operates like a solar inverter, acting as a current source to push real and reactive power onto the network.

In all modes of operation, the HV Terminal voltage is required to be present: the SST will not power up from the low voltage AC terminal or the low voltage DC terminal. With the high voltage terminal present, the SST can operate across all four power quadrants; without it, the SST will shut down to prevent backfeeding to HV.

STATCOM Operation

The Rectifier stage of the SST Topology 1 will sense secondary transformer voltage to extrapolate primary side voltage. SPEN will be able to control reactive power injection/absorption and voltage control two ways:

1. Setpoints for voltage deadband and reactive power injection slope
2. Reactive power setpoint

The first method mimics a traditional STATCOM operation. The two setpoints (deadband and slope) are highlighted in the Volt/Var curve shown in Figure A-6 .

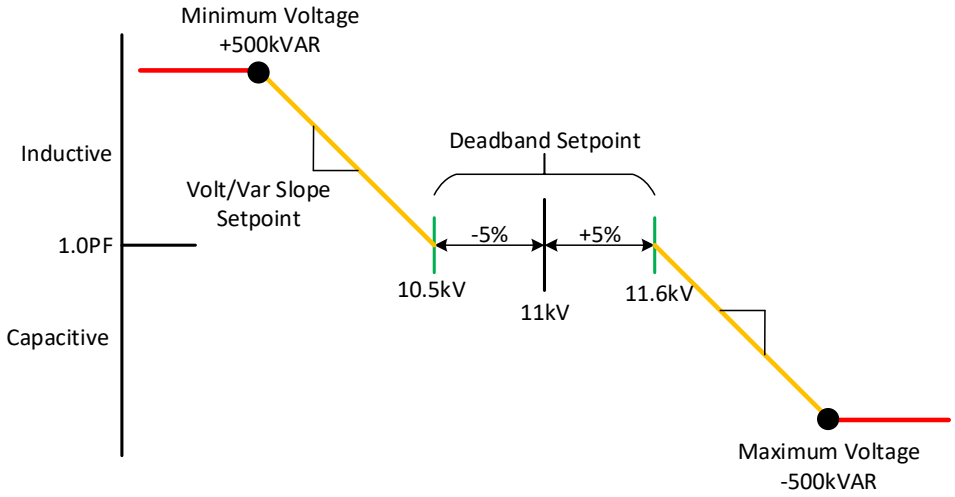


Figure A-6 STATCOM voltage vs reactive power operation

The maximum power rating of the rectifier module is 500kVA. With no other load on the rectifier, and full four-quadrant operation capability, up to 500kVAR can be produced for STATCOM operation. Thus, this is the limit presented at the top and bottom of the Y-axis at the red line. However, any other load on the rectifier (including the low voltage DC and AC modules) will limit this STATCOM capability. The SST will actively self-limit VAR output to within its operation range.

Furthermore, STATCOM functionality can only occur when the SST is under normal operation: if the SST is in standby, bypass, or conditional operation, no VAR will be injected into the grid. Thus, the volt/var slope and deadband setpoint should be carefully designed to operate within the -40% to +20% voltage operation range outlined for the rectifier and HV-T in A.1.1.

Overload Prioritizing

The rectifier module itself has been designed for 500kVA operation; yet, the rectifier loads and requirements are potentially much larger than the designed power rating. These power demands include 500kVA load at the low voltage AC terminal, 150kW at the low voltage DC terminal, and 500kVAR of STATCOM injection. To prevent unnecessary overload shutdowns, the rectifier must give priority to certain loads and ratchet back functionality in other areas.

The load priority is as follows:

1. LV-T AC Load
2. LV-T DC Load
3. HV-T STATCOM

If the low voltage AC and DC terminals combined are greater than 500kVA, all STATCOM operation at the HV-T will cease. If the load at the low voltage AC terminal by itself is greater than 500kVA, both the DC and STATCOM operation will cease. If the overload does not result in a fault, standby operation, bypass, or disconnection, the SST will continue to actively self-limit or immediately return functionality if power demand decreases.

A.1.5 4-Leg Topology

The SST creates a unique situation at the inverter stage for neutral handling: while 100% unbalance might exist at the output AC terminals, the specifications ask that none of this unbalance should be seen at the transformer. This challenge is described in four scenarios below.

Option 1 shows a direct connection between the transformer neutral and the SST output neutral terminal. Here, the SST could be fitted like a traditional transformer with a single neutral bushing, able to be grounded, with no impedance between transformer and SST neutral. While the wye to delta configuration of the traditional transformer should help eliminate the zero sequence element of any unbalance, it cannot fully guarantee a balanced current to the transformer and may even impact the operation of the SST by distorting the input currents.

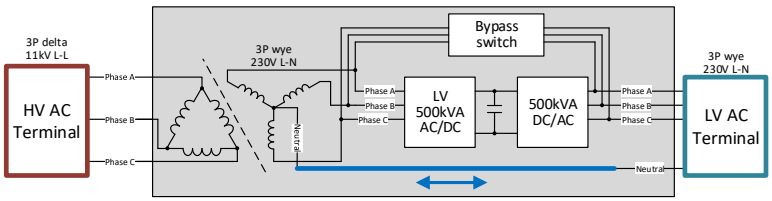


Figure A-7 Option 1: Direct connection between transformer and SST neutral bushing

Options 2 and 3 could guarantee balance at the transformer but forced separation between the input and output neutrals, leaving no path for the transformer neutral to be grounded. Option 2 also placed some stress on the internal DC bus: splitting the capacitors to create a midpoint now quadrupled the number of capacitors required to create an equivalent capacitance. It also threatens the stability of the rest of the system if a large neutral current causes these capacitors to go unbalanced and impacts the internal DC bus.

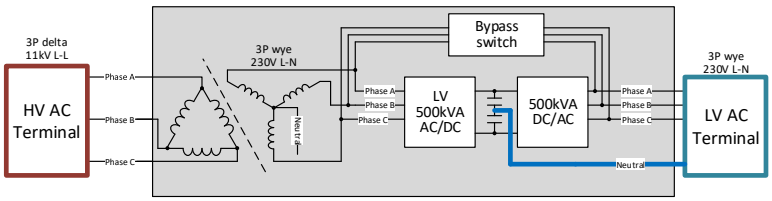


Figure A-8 Tie Neutral to DC bus mid-point

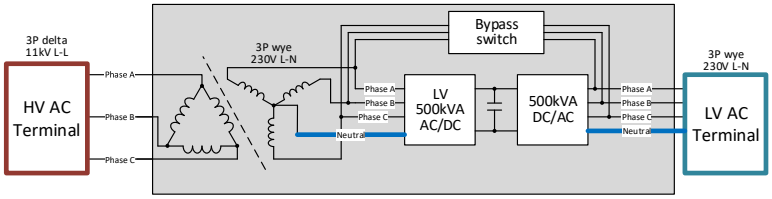


Figure A-9 Option 3: Neutral legs on both the rectifier and inverter stages

Therefore, we have chosen a "4-leg" topology for the inverter in option 4, as seen below. Here, two neutral bushings are still required to be able to measure the flow of neutral current for active control. However, these two terminals will be tied together internally and there will be no impedance between the neutral of the transformer and the output neutral of the SST. The neutral compensation algorithm senses the load neutral current and feeds an equal and opposite amount of current through the neutral leg, resulting in zero neutral current returning to the source delta-wye transformer.

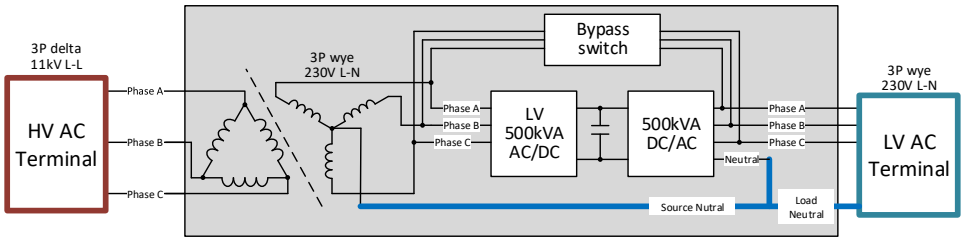


Figure A-10 Option 4: A neutral leg is added to the inverter to cancel unbalanced current

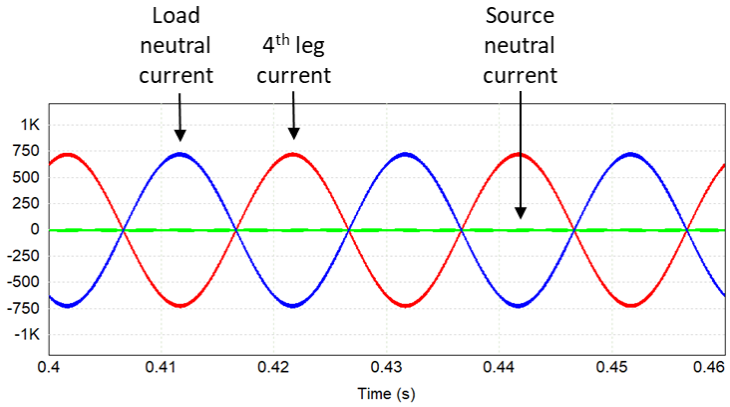


Figure A-11 Neutral current compensation

A.1.6 Individual Phase Control and Operation

The SST will offer unprecedented vision and control into the grid-edge of the network.

The inverter stage will capture and report the following real time grid values:

- L-N RMS Voltages the LV AC Secondary Terminal
- RMS current and phase angle at the LV AC Secondary Terminal
- Real Power (kW) magnitude and direction at the LV AC Secondary Terminal
- Reactive Power (kVAR) magnitude and direction at the LV AC Secondary Terminal
- Low Voltage Terminal Frequency
- Low Voltage Terminal THD

SPEN will be able to toggle and control in real time setpoints for the following parameters:

- LV Voltage Set Point for each phase (radial)
- LV AC Active Power setpoint (mesh)
- LV AC Reactive Power setpoint (mesh)

In a mesh network, each inverter phase will operate with independent current control so the P and Q setpoints on each phase can be any positive or negative value within the power capability of the system, shown in Figure A-12. Likewise, in a radial network the voltage setpoint on each phase can be any value within the capability of the inverter and the phase relationship can be adjusted as shown in Figure A-13. Note also the load profile of two phases of unbalanced, linear load and a third phase with a non-linear load. The inverter continues to maintain balanced three phase voltage for each of these loads.

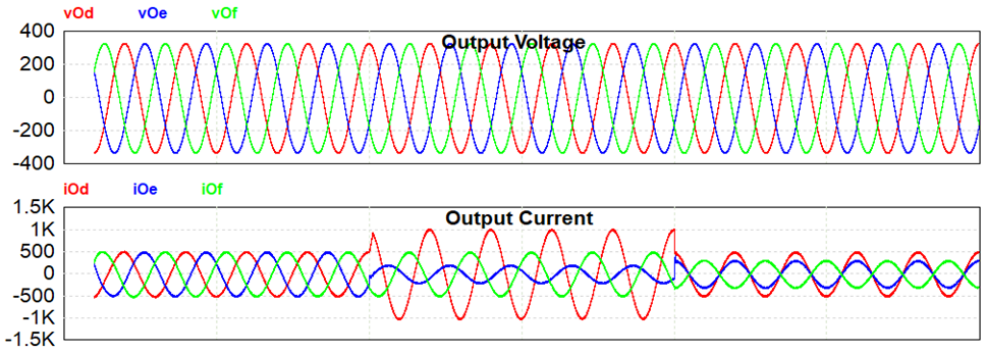


Figure A-12 Unbalanced output currents in mesh operation

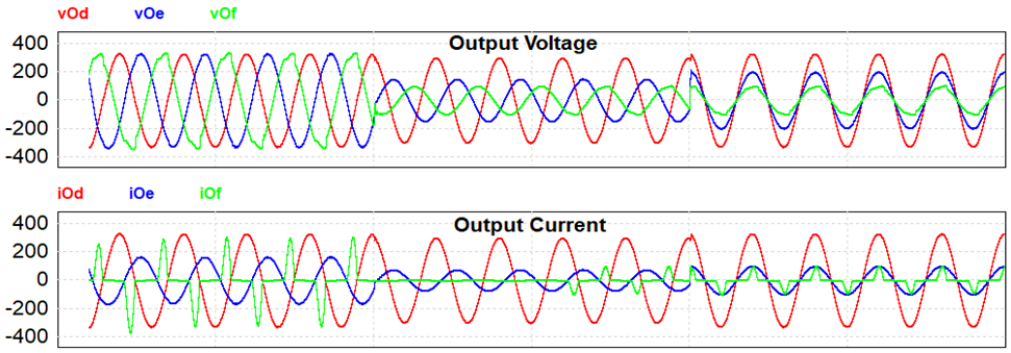


Figure A-13 Unbalanced output voltages in radial operation

A.2 Rectifier and inverter hardware

As the input delta-wye transformer is relatively flexible depending the supplier, this document will focus on the design of the power electronics after the delta-wye transformer. The maximum operating conditions for the rectifier and inverter are shown in Table A-7 and drive the selection of hardware components. Because the rectifier and inverter current and voltage stresses are very similar, the component selection will be identical between the rectifier and inverter.

Table A-7 Rectifier and inverter maximum operating conditions

Rectifier max voltage (RMS)	**541V L-L (312V L-N)**
Rectifier max current (RMS)	920A
Inverter max voltage (RMS)	478V L-L (276V L-N)
Inverter max current (RMS)	942A

A.3 Rectifier and Inverter LC filter design

The LC filter design is based around the switching frequency (20kHz) of the devices and the current handling requirements of the system. The general rule of thumb is to aim for an LC filter cutoff of less than 1/10th of the switching frequency, which translates to less than 2kHz. While there are infinite combinations of L and C values that can achieve a 2kHz cutoff, there are some realities of implementation that drive L and C to a certain ballpark range.

A minimum L value is needed to ensure current ripple is not so high that it becomes detrimental to current THD as well as high inductor core losses. The upper end for the L value is limited by what is practically achievable in the available space. Based on discussions with suppliers and simulation results, the design team settled on 200uH as a suitable balance between current THD performance and a manufacturable inductor. Each inductor will handle 400Arms nominal and be spec'd for inductance stability up to 600Arms (850Apk) to account for unknown grid events.

The capacitor will be the following 50uF AC capacitor with 4 in parallel for an equivalent capacitance of 200uF. The LC combination of 200uH and 200uF produces a cutoff frequency of 796Hz, which is well below 1/10th of the switching frequency. From a current handling perspective, the capacitors should see less than 5A @ 50Hz each, so their 23A rating provides plenty of margin. There is an expandable safety disconnector near the terminals in the case of overpressure.

A.4 Paralleling methodology

The rectifier and inverter devices will need to be in parallel to achieve the desired current handling. When paralleling devices, the most important requirement is to ensure thermal and current balance. The following parallel methodology was processed.

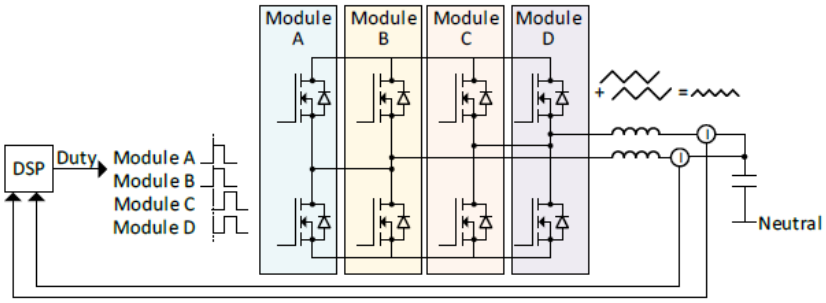


Figure A-14 Parallel methodology for a single rectifier/inverter phase

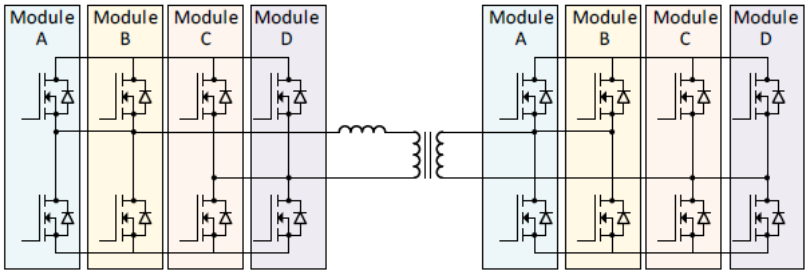


Figure A-15 Parallel methodology for DAB

As seen in both Figure A-14 and Figure A-15, directly in parallel as are modules C&D. This is referred to as hard paralleling. In order to ensure current balance in hard paralleled modules, the DC bus bar must be routed to force equal current flow between the modules to the bypass capacitor as shown in Figure A-16. Next, the gate drive signals between A&B and between C&D must not have any timing differences. This can be achieved by simply driving each module with the same gate signal, ensuring that the gate driver can supply enough sink/source current to the gate of the device.

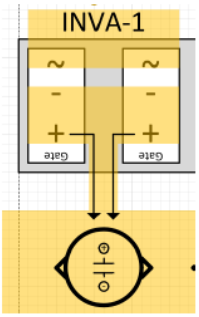


Figure A-16 Hard paralleling busbar design

As Figure A-15 shows, in the rectifier/inverter, the combinations of A&B and C&D are then paralleled after the inductor. Current sensors will be placed on each inductor so that the DSP can control balance between the inductors. A further benefit with this method is that A&B can be interleaved with C&D to reduce ripple currents on the output, minimizing THD.

In the DAB, A&B forms one leg of the full bridge and C&D form the other leg. Since both the rectifier/inverter and DAB contain 2 sets of hard paralleled modules, the hardware assemblies are identical and can be shared – this includes the cold plate, devices, and gate drive. The connection of magnetics and other passive components as well as controls will be what makes the DAB different from the rectifier/inverter.

A.5 Auxiliary Designs: Pre-Charge Circuit, Internal Power, Control Board

While a majority of the design focus has been on the operation of each module, several auxiliary components are required for the safe startup and operation of these features. Notably, the large bulk capacitance of the internal DC bus can cause large bursts of inrush current during turn-on if not pre-charged and handled correctly.

Another element tied to this pre-charge circuit is the auxiliary power supply. The SST power supply must power all internal sensors, controllers, communication, and gate drivers for the SST. Therefore, it must be rated to handle isolation requirements, thermal limits, and the wide voltage operation range. The voltage requirements of the auxiliary power supply will determine the undervoltage handling of the entire SST. EGB is working to find a suitable off-the-shelf supply that meets all of the SST requirements while not diverting the EGB engineering design team.

Finally, the control board serves as a central point of command for taking in sensor values, performing calculations, and outputting commands. It will also perform grid monitoring, initiate protection measures, monitor temperatures, and control pre-charge, bypass, and protection relays.

A.5.1 LV-SST Pre-charge circuit

The pre-charge circuit is implemented to charge the bulk DC-link capacitor during start-up to a suitable voltage level before operating the power electronics. This circuit is required to prevent large uncontrolled inrush currents from flowing through the SiC body diodes, likely causing device failure. The proposed pre-charge sequence is as follows, referencing Figure A-17.

1. The 50Hz traditional transformer is energized via 11kV line-to-line voltage source.
2. The 50Hz traditional transformer will immediately energize the Normally Open 4 (NO4) contactors to bypass the LV-SST. This immediate energization without the DSP controller intervention is possible since the Normally Closed 4 (NC4) contactors are connected in series with NO4 control coils and transformer sources. Furthermore, the NO4 contactors are energized only when the 50Hz transformer is energized, which prevents a potential back-feeding. Back-feeding is defined as energization of the delta-wye transformer from the load side without an 11kV voltage source present.
3. The 50Hz transformer also powers the auxiliary power supply that powers the DSP controller. The DSP controller starts a contactor control sequence.

4. The DSP controller closes the Normally Open 1 (NO1) contactor. The DC-link capacitor is charge through a separate three-phase rectifier, a resistor, and NO1 contactor. The rate of DC-link voltage change is based on the in-series resistance and DC-link capacitance.
5. When the DC-link voltage has reached a predefined voltage threshold which will be determined later, the DSP controller closes the Normally Open 2 (NO2) and Normally Open 3 (NO3) contactors. It should be noted that the power sources of the NO1, NO2 and NO3 contactor control coils should not be directly derived from the transformer to prevent accidental contactor operation during a brief transformer voltage dropout.
6. SST starts operation to match the load current with the inverter current output. After the currents are matched, which brings the current through the NO4 contactors to near zero, the DSP controller opens NO4 contactors via NC4 contactors. This ends the startup sequence.

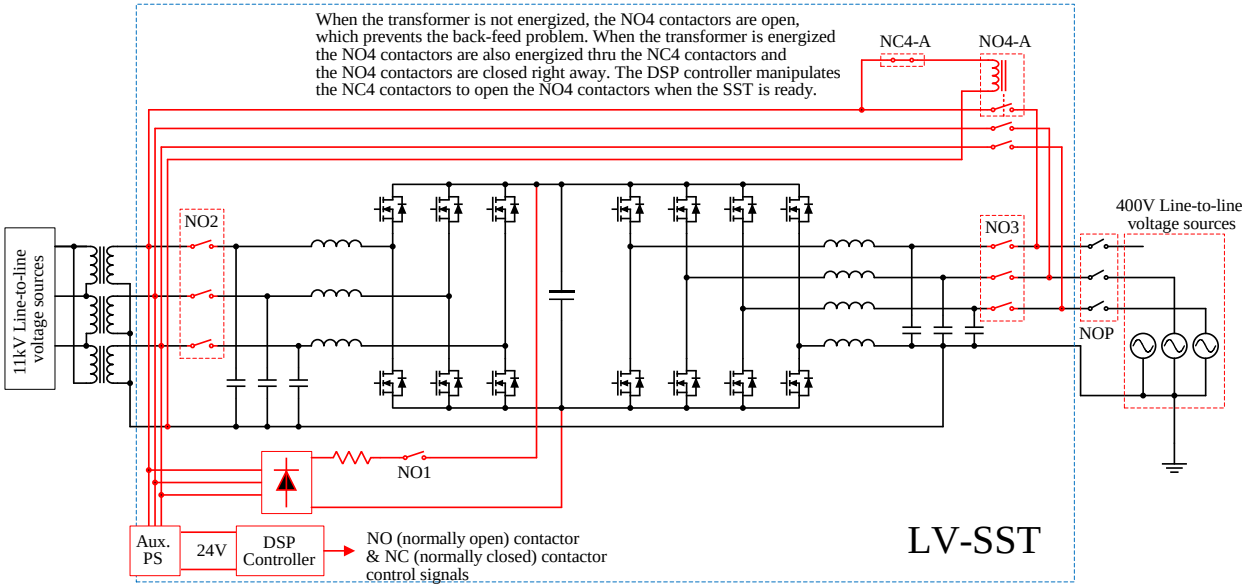


Figure A-17 pre-charge and bypass contactors

A.5.2 System (Auxiliary) Power Supply

The system power supply must provide long term reliability, resiliency during fault conditions and wide input voltage range. This input voltage range must extend beyond the input voltage range of the SST itself to ensure stable operation during fault conditions. To enhance reliability and resiliency, the power supply will be capable of providing 25-50% more output power than the SST requires in normal operation. The 3kV RMS isolation requirement requires a 3-phase isolation transformer be inserted between the power supply input and the input voltage source.

A prime example of a high quality power supply that meets the stated requirements is the PULS QT20.241 model. This passively cooled 480W power supply can provide up to 720W for 4 seconds and can optionally be configured in a 1:1 redundancy scheme further enhancing resiliency.

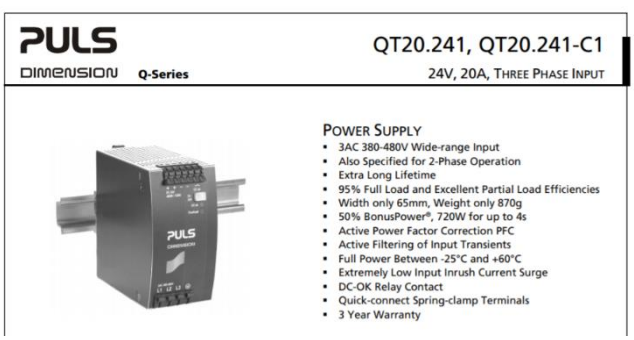


Fig. 3-1 **Input voltage range**

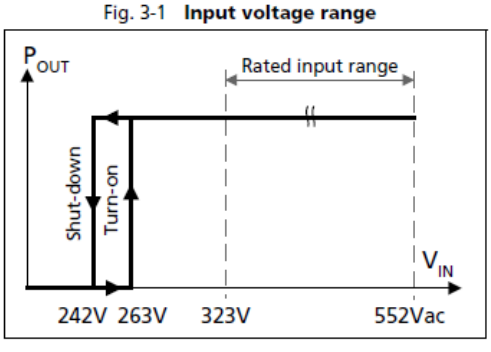


Figure A-18 Auxiliary power supply considered for the SST

A.5.3 Control and Sensor Module

The Silicon Carbide Control and Sensor module (SiCSM) contains a DSP to sense current and voltage and control the Power Electronics, plus a general-purpose microcontroller that manages the entire system, including local & remote communications. All I/O to the SiCSM must be SELV and galvanically isolated before being presented to the SiCSM. Please see Modular SiC Control and Sensor Module (SiCSM) Hardware FUSP (Document Number: 201-000005-00-A) attached at the bottom of this document for further design information.

Sensor Locations

The voltage and current sensors for control and grid monitoring are required in the following locations of the SST.

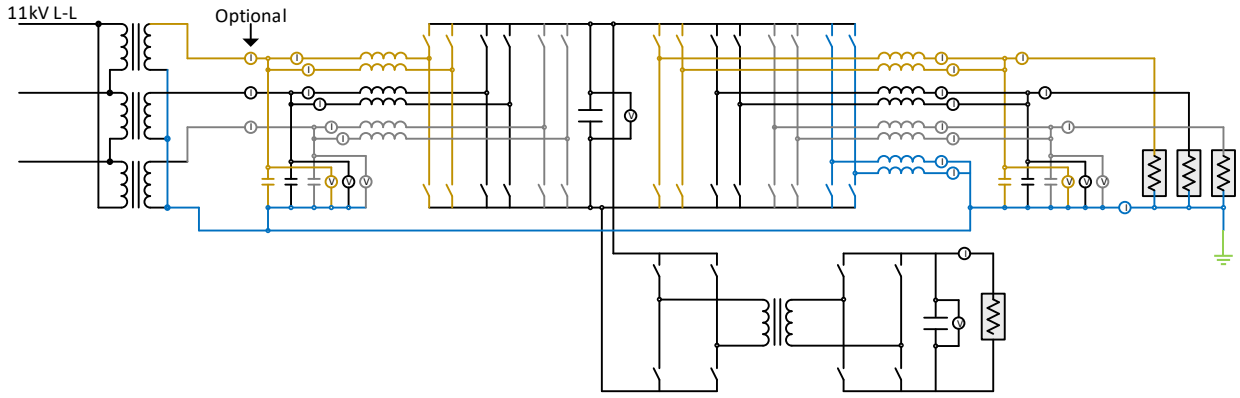
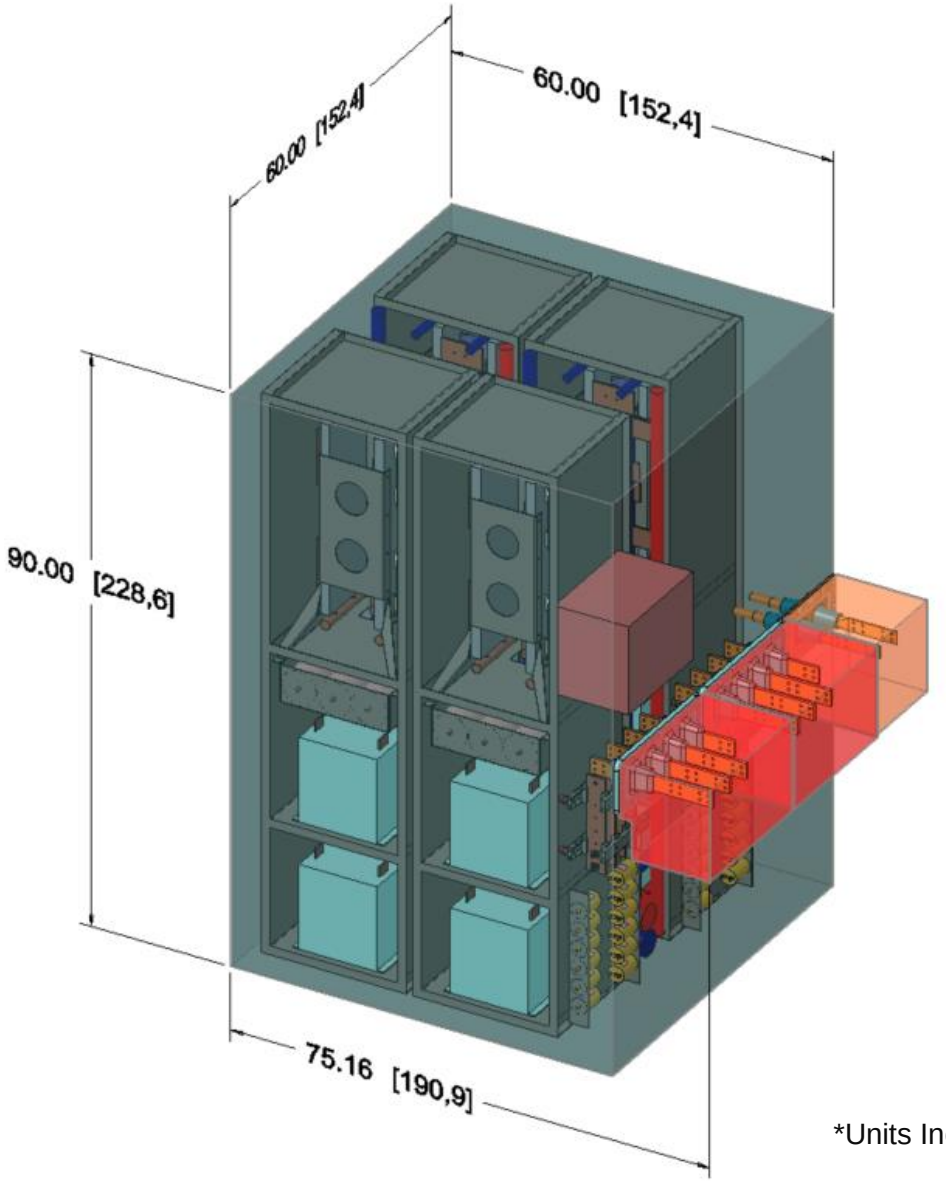


Figure A-19. SST Topology 1 current and voltage sensor locations

In both voltage and current sensing, there is a concern with minimising noise pickup due to the high power switching environment of the SST. To deal with this issue, the control board that houses the DSP and ADCs will be physically located very close to the voltage and current sensors to minimize sensing cable lengths. There will be two control boards in the SST; one to control the rectifier/inverter and another to control the DAB. Both control boards will be identical and will communicate with each other via CAN messages.

A.6 Mechanical Design

Based on initial mechanical design, size of the current concept is 152cm (60”) square and 228 cm (7’) tall not including the bushing boxes. The system is mainly comprised of four quadrants, one per phase of a three-phase system, and a fourth that handles the neutral current control for phase balancing, and the 950VDC service port. This modular high-level structure is shown below in Figure A-20 where the outer enclosure is semi-transparent and the orange boxes at the front hold the input and output bushing boxes.



*Units Inches [Centimetres]

Figure A-20 LV-SST Topology 1T Electronics Mechanical Layout

Each of the four quadrants (sub-assemblies) are designed to be independently built and tested before final assembly. This simplifies construction by repeating and reusing similar assemblies. This flexibility will be leveraged for product variants in the future.

EGB will work closely with our Dyersburg manufacturing team to create detailed drawings for assembly and test. The layout includes not only electrical and thermal considerations, but also assembly order, lift points, wire bend radius, and tool access. Here, the team has achieved a high density while balancing the space needed for cable routing, water cooling, bracketing, and isolation standoffs.

Each sub-assembly in Figure A-21 houses the rectifier and inverter of a single phase. The neutral inverter phase and DC/DC stage are combined into the fourth tower. The input and output bushings are both connected to the front face with the input and output AC filter capacitors mounted immediately below and the bypass contactor mounted directly above. For reference, Figure A-22 shows the LV-SST topology.

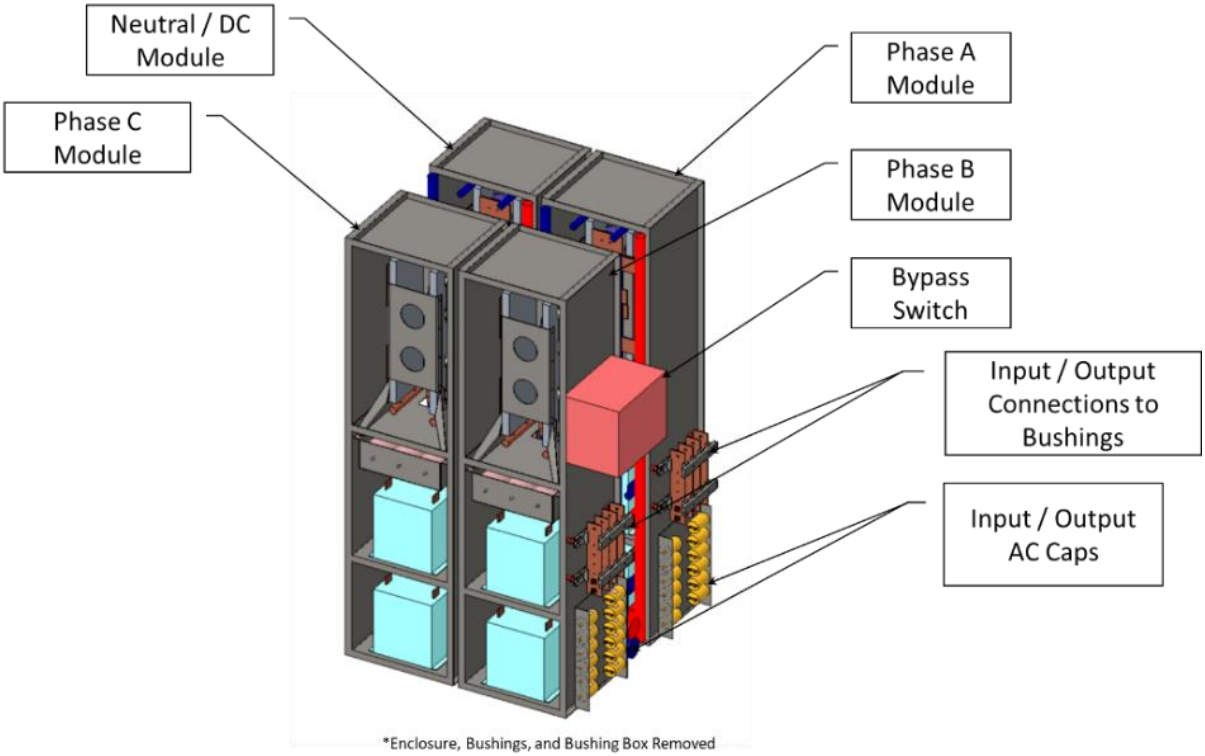


Figure A-21 LV-SST mechanical layout

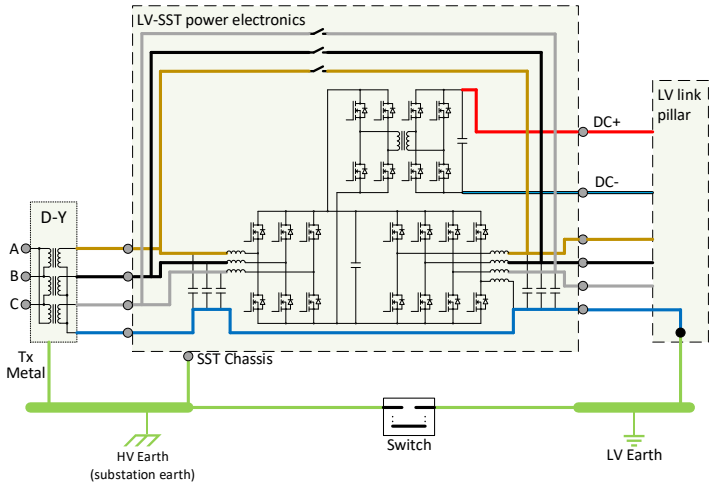


Figure A-22 SST Circuit topology

Figure A-23 shows a detailed capture of a single quadrant. Each sub-assembly houses the silicon carbide modules, inductors, DC capacitors, laminar bus bars, and liquid cold plates. For reference, Figure A-24 shows this circuit topology.

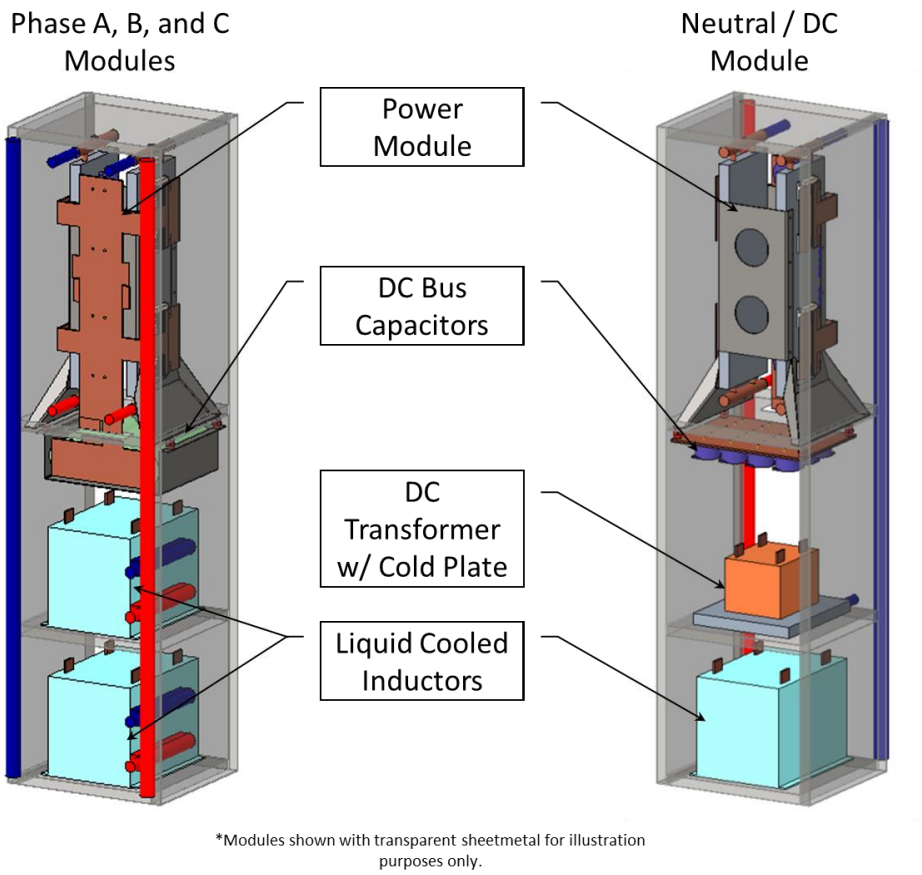


Figure A-23 Mechanical model of each phase (left) and neutral/DC (right) sub-enclosures

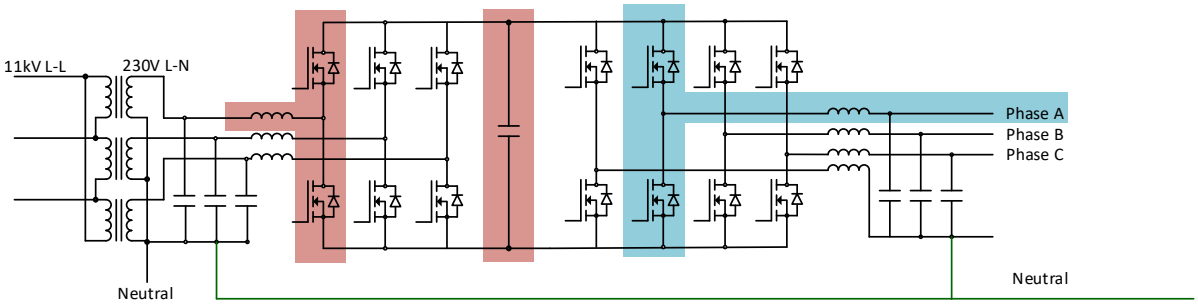


Figure A-24 Electrical components housed in each phase sub-enclosure

The power module at the top of the sub-assembly is composed of four SiC modules mounted on a water cooled heatsink shown in Figure A-25. Two of these heatsinks are placed in parallel and a laminated DC bus bar forms a “U” shape linking the two sides while supporting capacitors in the middle. For reference, Figure A-26 shows this circuit topology.

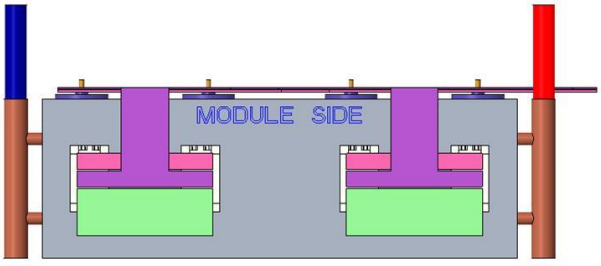


Figure A-25 Power Module Assembly

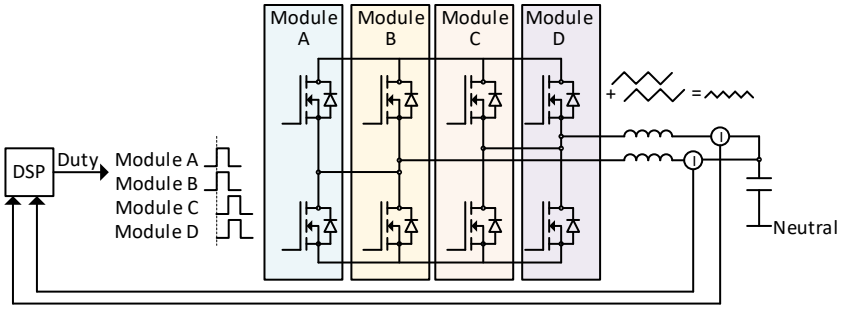


Figure A-26 Parallel method for each inverter leg

Each cold plate supports enough SiC for a single phase: four modules in parallel. The bus bars directly connect two modules in hard parallel to match impedance and split the current as equally as possible. These two sets of hard paralleled modules are then interleaved and paralleled via the inductor filter output, housed just below. The mechanical subassembly is shown in Figure A-27 below.

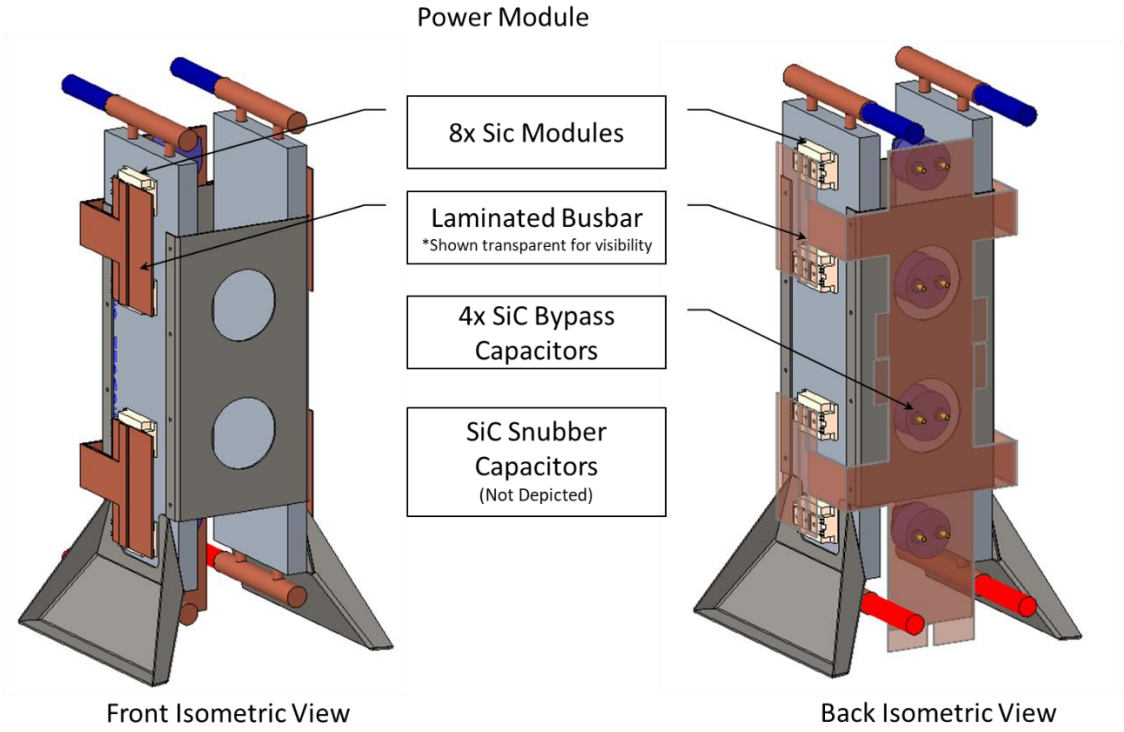


Figure A-27 Power Module Mechanical Structure

A.6.1 Key Technology & Supply Chain Partners

Table A-8 shows key technology and supply chain relationships established to date. The top three are the most well established with the last two being much earlier in the process and the middle three somewhere in between.

Table A-8 Key Technology Partners

Key Technology	Partner	Current State	Next Steps
SiC Modules	Infineon	Analysis & Simulation Complete	PO & Design into HW
DC & AC Capacitors	Cornell Dubilier TDK/EPCOS	Analysis & Simulation Complete	PO & Design into HW
High Power Inductors	CTM Magnetics	Analysis & Simulation Complete	PO & Design into HW
SiC Liquid Cold Plates	Mersen ACT	Early Engagement Identified	Analysis & Selection
High Current Bussing	Mersen	Early Engagement	Analysis & Selection
High Pwr. & Freq Trans	muRata, HiMag, Datatronics	Quoting Design Requirements	Analysis & Selection
System Level Thermal Management	ACT Mersen	Identified Early Engagement	Engage and Analyse
Thermal Analysis Tool	SimScale	4 Wks. Actively Using	Start with the SiC Cold Plate Analysis

A.7 Thermal Management

A.7.1 Expected Losses

Table A-9 shows preliminary estimates of the expected worst-case heat load to be managed by the water-cooling system. The table is divided into three subsystems AC, DC Service and equipment common to the complete system. This data will be used to size individual component cooling and the system level heat exchanger.

Table A-9 Expected Component Thermal Losses

Subsystem Component	Component Description	Component Heat Load (watts)
Back/Back AC to AC	SiC Module: 4 Paralleled @ 182A each	455
	AC Inductor: 200uH@400A	620
	Gate Driver – UCC21750	2
DC to DC Service	DC Transformer & Inductor: 0.4% of 200kVA	800
	SiC Module	480
	Gate Driver – UCC21750	2
Common Equipment	Aux PS: Puls 95% @ 500W	25
	SiCSM + Sensors	10
	Losses (0.5%): System Interconnects	2,500
	Bypass CB – Schneider NW40	650
	Disconnect Relays	500
	Heat Exchanger: Liquid Pump(s) + Fan	1,250
	Misc. & Unknowns	100

A.7.2 Liquid Cooling Method

The cooling methods required of a 500kVA power electronics system are not without much complexity and trade-offs. The team along with our key technology (SiC, Magnetics) partners analysed various cooling methods, in the final evaluation, the heat load requires a high level of cooling to maintain safe operating margin for a 500kVA (plus 30% overload capacity as required) power electronics system and liquid cooling was selected. Forced air and passive liquid cooling was also considered, which was assumed to be sufficient at the time the proposal was written.

- Passive liquid cooling for the expected heat load is approximately 30-50% larger, and the internal electrical layout presents additional technical risks due to this size and proportions and does not have the thermal performance to handle bursts of power/heat required during overload cases.
- Forced air cooling confined inside a structure without open air, the SST external fins would need to have access to the cooler external air via a ducted active circulation system.

The design constraint for maintenance free or very low maintenance without special tools/training is critical and will be followed throughout the design process. A circulation of water + stabilizer that serves to lower the freezing point and be a corrosion inhibitor is assumed. This will require a remote mounted heat exchanger (like an auto radiator) with a speed-controlled fan and a liquid pump. This approach is quite typical in modern, large power electronics systems.

Thermal Conductivity is the key when looking at cooling methods. Air whether it is free or forced, has low thermal conductivity. Thermal conductivity refers to the ability of a substance to transfer heat. Here are thermal conductivity ratings of some common materials (measured in Watts per meter-degree Kelvin; W/m-K).

- Air 0.026
- Styrofoam 0.029
- Wood 0.11
- Water 0.61
- Glass 0.8
- Concrete 1.0
- Steel 46
- Aluminium 240
- Copper 400

It is striking to see that water is 23.5 times more efficient in transferring heat than air. Further, given a specific volume of water flow over a hot component (the volumetric flow rate), water has a heat carrying capacity nearly 3,500 times that of air. This is illustrated in Figure A-28 below. An air cooled three phase inductor releases 3kW into the surrounding air whereas a liquid cooled design of the same power rating releases 90W. The balance of the heat is transferred to the cooling liquid and removed by the remote located heat exchanger.

The SST will use aluminium (or copper) and not steel wherever mechanical structure and heat transfer is considered critical to the resiliency of the system.

Figure A-28 Liquid vs. Air Cooled Magnetics

Aluminium liquid cooling plates with embedded tubing and attached manifolds to cool the SiC Modules, an example shown in Figure A-29, is critical in maintaining safe operating margin for advanced switching

devices. The coolant tubing is located directly below the mounting surface of the SiC module providing the most direct path to manage the generated heat.

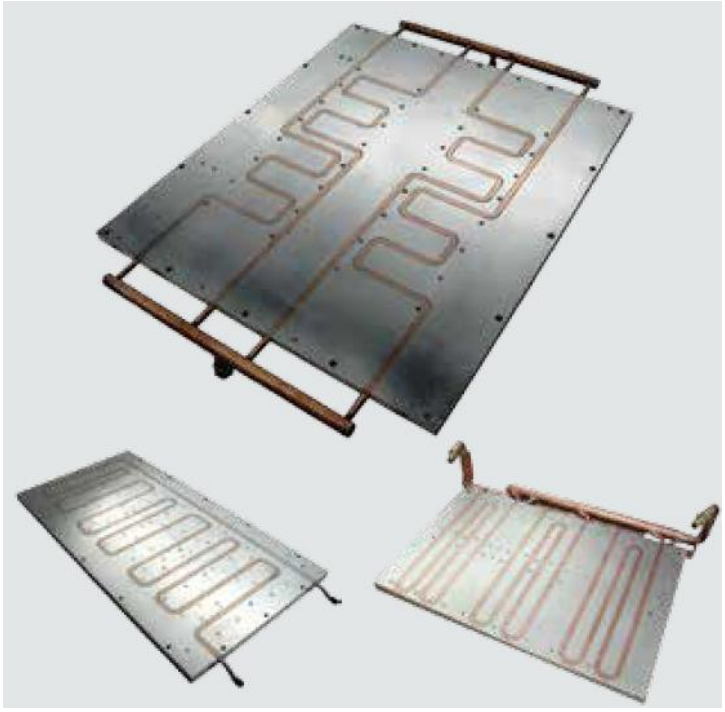


Figure A-29 Examples of SiC Liquid Cold Plates

Liquid cooling pipes within each quadrant will be combined into an overall system manifold which exits the overall enclosure leading to the remotely located heat exchanger as shown in Figure A-30 below using the red and blue pipes. This heat exchanger can be located either external to the SPEN substation structure or mounted to the interior of an external wall, allowing the warmed air to directly exit the substation structure. The design decision for the location of the heat exchanger will be tightly coupled with SPEN requirements and openly discussed going forward.

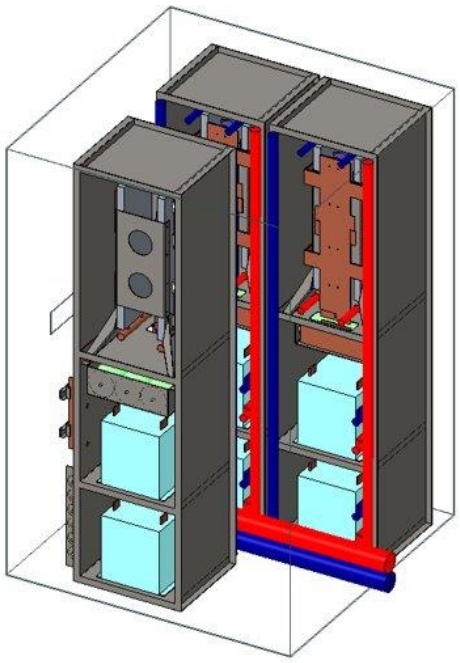


Figure A-30 System Level Liquid Cooling Pipes

A.7.3 Thermal Sensing and Monitoring

The system will be equipped with thermal sensors located in all the thermally critical locations of the system:

- SiC Modules (multiple)
- Magnetics (multiple)
- DC & AC Capacitors (multiple)
- Coolant liquid (multiple) at critical locations
- Ambient air (multiple) inside the enclosure
- Air external to the enclosure (multiple)

These sensors will periodically report temperature readings in real-time up to the SiCSM where a high-priority thermal management algorithm runs in real time. This algorithm will manage the available power for the entire system and communicate this status to the SPEN System Control function. A resilient hardware driven thermal overload function will exist that can shut down the system, avoiding hardware damage to the power electronics in the event of a software/firmware failure.

Appendix B Demonstration of operation of SST Topology 1 (UPFC building block) in Radial and Meshed network

B.1 Radial Network Scenarios Provided by SPEN

A summary of the Radial Network test scenarios considered for simulation and analysis shown in Table B-1. EGB used PSIM simulation package to model and simulate the SST Topology 1 operation under these conditions, the results are provided in the body of this section.

Table B-1 Radial Network Scenarios

Scenario	LV Input Voltage (% nominal voltage=400V L-L)	Total AC Load	Total DC load	Target LV output Voltage (% nominal voltage=400V L-L)	Target imbalance seen by Trans. (%)	Target power factor seen by Trans.
1	0.94	500kVA, pf=0.97 lag Imbalance= 0.0%	0	1.1	0	0.97 Lag
2	0.94	500kVA, pf=0.97 lag Imbalance= 0.0%	0	1.1	0	1
3	0.94	500kVA, pf=0.97 lag Imbalance= 30.0%	0	1.1	0	1
4	0.94	350kVA, pf=0.97 lag Imbalance= 30.0%	150kW	1.1	0	1
5	1.1	500kVA, pf=0.97 lag Imbalance= 0.0%	0	0.94	0	0.97 Lag
6	1.1	500kVA, pf=0.97 lag Imbalance= 0.0%	0	0.94	0	1
7	1.1	500kVA, pf=0.97 lag Imbalance= 30.0%	0	0.94	0	1
8	1.1	350kVA, pf=0.97 lag Imbalance= 30.0%	150kW	0.94	0	1
9	1.1	500kVA (reverse power export to conventional transformer) pf=0.97 lead Imbalance=0.0%	0	0.94	0	1
10	1.1	500kVA (reverse power export to conventional transformer) pf=0.97 lead Imbalance=30.0%	0	0.94	0	1
11	1.1	350kVA (reverse power export to conventional transformer) pf=0.97 lead Imbalance=30.0%	150kW	0.94	0	1

Figure B-1 illustrates the network configuration for various Radial scenarios, and Figure B-2 illustrates the UPFC configuration with power measurement points. Total of five points are selected as the measurement points as follows.

1. Source – SST Topology 1 input
2. Middle – Power flow as defined as $S_{middle} = V_{source} * I_{load}$.
3. Load – UPFC output
4. Shunt inverter
5. Series inverter
6. DC/DC converter load

A power constant load is used as the local load, and a resistive element is used as the DC load.

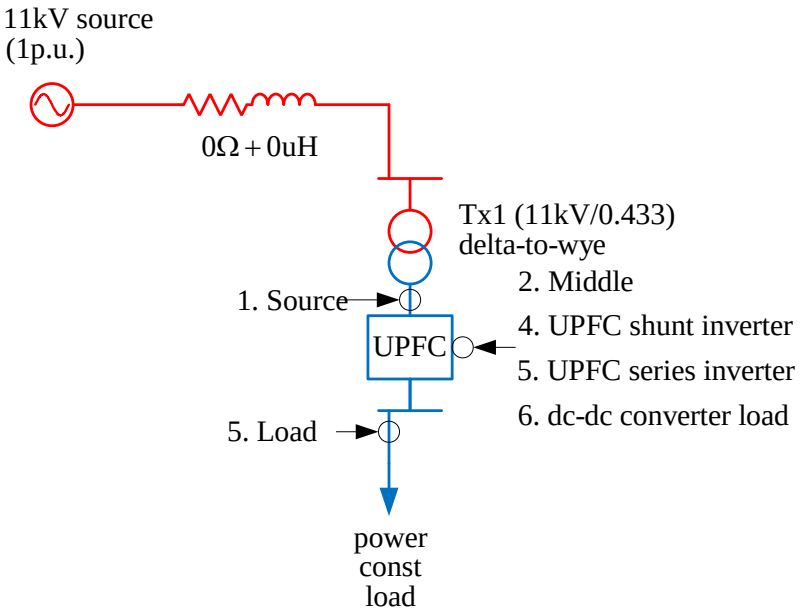


Figure B-1 Network configuration consider for demonstration of SST Topology 1 (UPFC design) operation in radial network

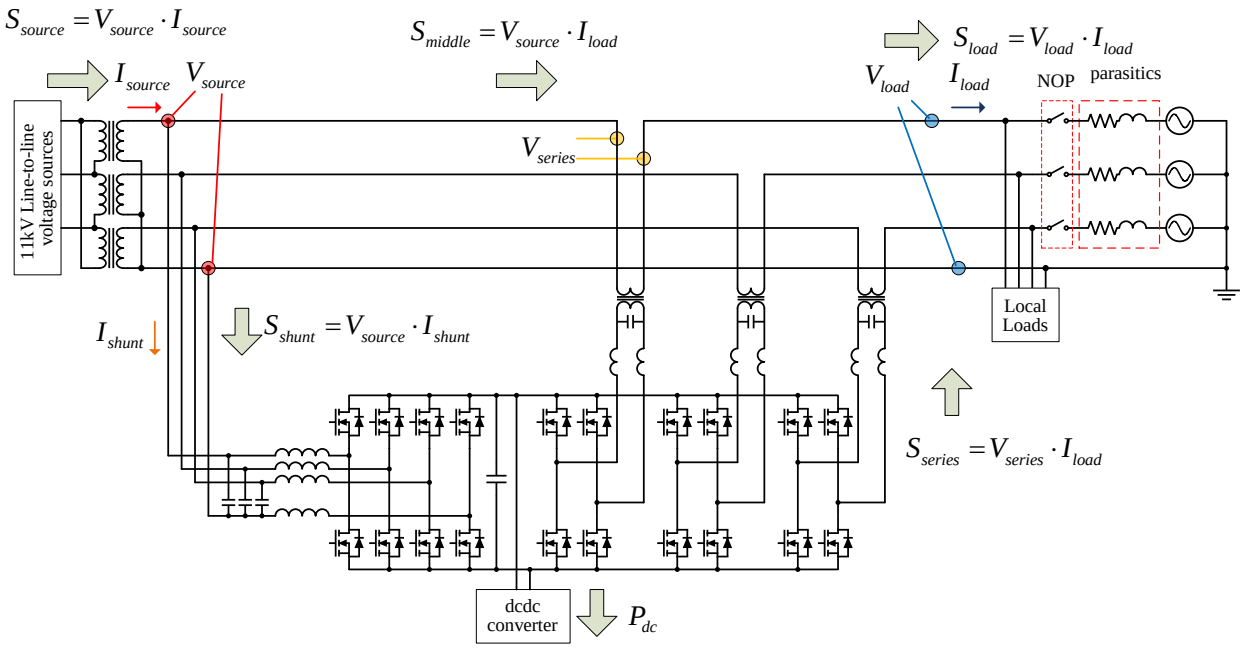


Figure B-2 SST Topology 1 configuration with power measurement points

B.1.1 Scenario 1

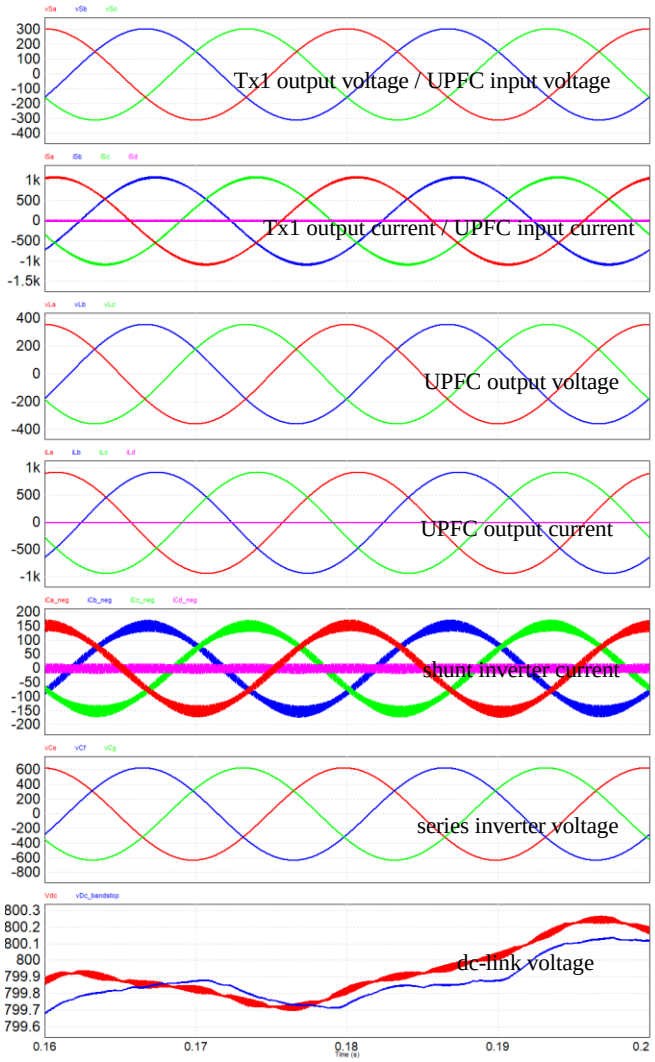


Figure B-3 Scenario 1 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-2 RMS measurements

	Phase A	Phase B	Phase C	Neutral
Input voltage	217	217	217	
Input current	762	762	762	6.7
Output voltage	254	254	254	
Output current	656	656	656	0
Shunt current	107	107	107	6.7
Series voltage	444	444	444	

Table B-3 Scenario 1 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
1. Source	165	162	0.978	165	162	0.978	165	162	0.978	496	485
2. Middle	142	138	0.972	142	138	0.972	142	138	0.972	427	415
3. Load	166	162	0.97	166	162	0.97	166	162	0.97	500	485
4. Shunt	23	23	1	23	23	1	23	23	1	70	70
5. Series	24	23	0.956	24	23	0.956	24	23	0.956	73	70
6. DC load											0

Figure B-3 illustrates the SST Topology 1 input and output voltage and current, shunt inverter current, series inverter voltage, and DC-link voltage of scenario 1, and its RMS measurements are given in Table B-2.Table B-3 summarises the apparent power, real power and power factor of scenario 1.

The series inverter of the SST Topology 1 generates the voltage difference between the source voltage and desired output voltage reference voltage. The shunt inverter is then responsible for compensating any unbalanced current from loads and inject reactive power to match the desired PF at the transformer terminal (i.e. input). Scenario 1 calls for 0.97 PF at both input and output; therefore, the shunt inverter does not need to generate any reactive power, and the shunt inverter only supplies the active power required to increase the UPFC output voltage by the series inverter.

B.1.2 Scenario 2

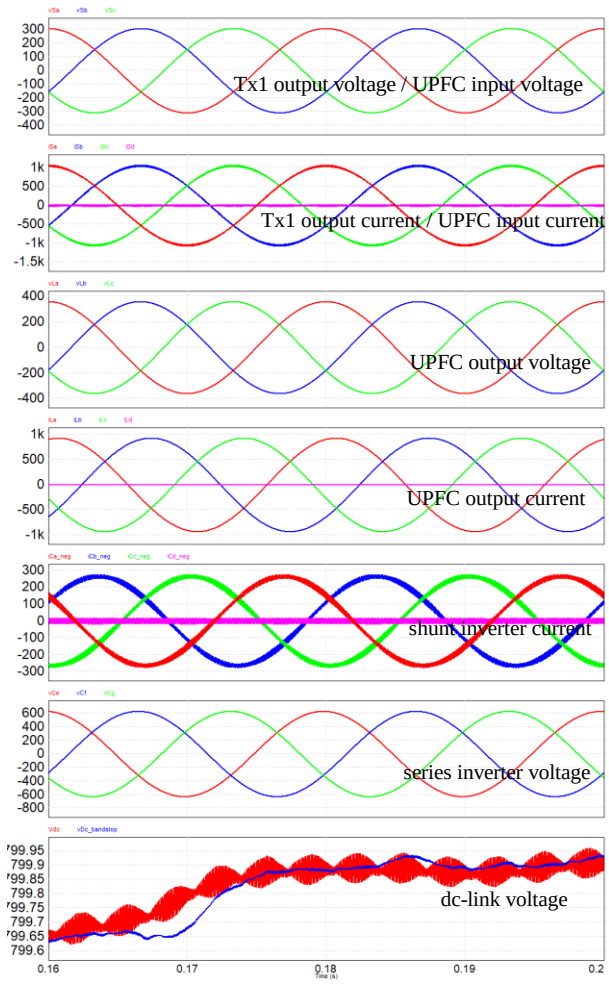


Figure B-4 Scenario 2 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-4 RMS measurements

	Phase A	Phase B	Phase C	Neutral
Input voltage	217	217	217	
Input current	746	746	746	7
Output voltage	254	254	254	
Output current	656	656	656	0
Shunt current	186	186	186	7
Series voltage	444	444	444	

Table B-5 Scenario 2 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
1. Source	162	162	1	162	162	1	162	162	1	485	485
2. Middle	142	138	0.972	142	138	0.972	142	138	0.972	427	415
3. Load	166	162	0.97	166	162	0.97	166	162	0.97	500	485
4. Shunt	40	23	0.57	40	23	0.57	40	23	0.57	121	69
5. Series	24	23	0.95	24	23	0.95	24	23	0.95	73	69
6. DC load											0

Figure B-4 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 2, and its RMS measurements are given in Table B-4. Table B-5 summarizes the apparent power, real power and power factor of scenario 2.

The scenario 2 is very similar to the scenario 1. The only difference is that the target power factor seen by the transformer is changed from 0.97 to 1.0. The shunt inverter corrects the PF to be 1.0, which increases its reactive power consumption. Other conditions remain similar.

B.1.3 Scenario 3

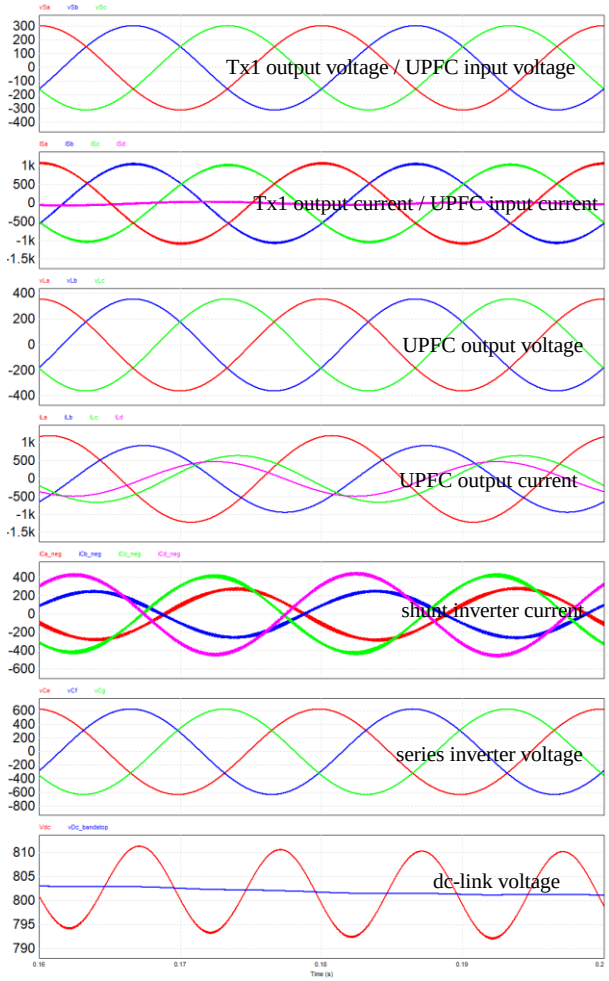


Figure B-5 Scenario 3 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-6 RMS measurements

	Phase A	Phase B	Phase C	Neutral
Input voltage	217	217	217	
Input current	745	745	745	7.6
Output voltage	254	254	254	
Output current	852	656	459	340
Shunt current	215	187	317	340
Series voltage	444	444	444	

Table B-7 Scenario 3 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
1. Source	161	161	1	161	161	1	161	161	1	485	485
2. Middle	185	180	0.972	142	138	0.972	100	97	0.972	427	415
3. Load	216	210	0.97	166	161	0.97	116	113	0.97	500	485
4. Shunt	47	-18	-0.39	41	23	0.57	69	65	0.94	156	69
5. Series	32	30	0.95	24	23	0.95	17	16	0.95	73	70
6. DC load											0

Figure B-5 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 2, and its RMS measurements are given in Table B-6. Table B-7 summarises the apparent power, real power and power factor of scenario 3.

The change in the scenario 3 from the scenario 2 is the significant load imbalance, in which the phase A, B, and C are 130%, 100% and phase 70% of the average currents of all three phases. All the imbalance is corrected by the shunt inverter, and it should be noted that the neutral is most heavily loaded.

B.1.4 Scenario 4

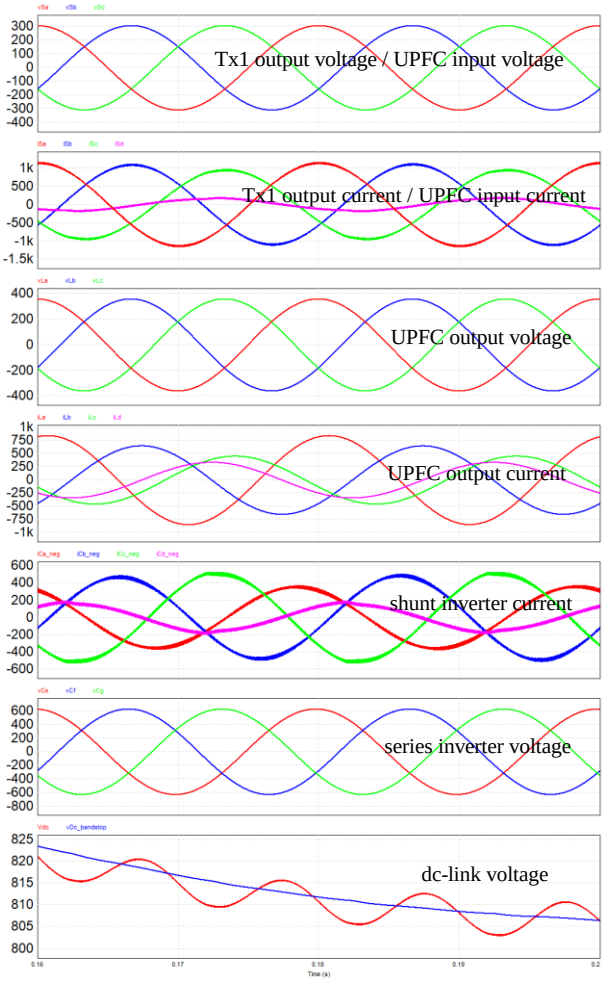


Figure B-6 Scenario 4 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-8 RMS measurements

	Phase A	Phase B	Phase C	Neutral
Input voltage	217	217	217	
Input current	803	774	672	121
Output voltage	254	254	254	
Output current	596	459	321	238
Shunt current	252	339	363	118
Series voltage	444	444	444	

Table B-9 Scenario 4 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
1. Source	174	174	1	167	167	1	145	145	1	486	486
2. Middle	129	126	0.972	100	97	0.972	70	68	0.972	299	290
3. Load	151	147	0.97	117	113	0.97	82	79	0.97	350	240
4. Shunt	54	481	0.88	72	70	0.965	78	78	0.99	205	196
5. Series	22	21	0.95	17	16	0.95	12	11	0.95	51	48
6. DC load											154

Figure B-6 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 4, and its RMS measurements are given in Table B-8. Table B-9 summarises the apparent power, real power and power factor of scenario 4.

The loads in scenario 4 is also imbalanced as is in scenario 3, but the ac load is reduced from 500kVA to 350kVA, and the dc port is loaded with 150kW. This creates the peak phase current of shunt inverter to be over its rated current, which is at about 500A and it is about 350A RMS current. The over current occurs on phase C, and the phase C current is limited in sinusoidal format. This leads to less imbalanced correction, which can be observed by the non-zero neutral current at the transformer terminal.

B.1.5 Scenario 5

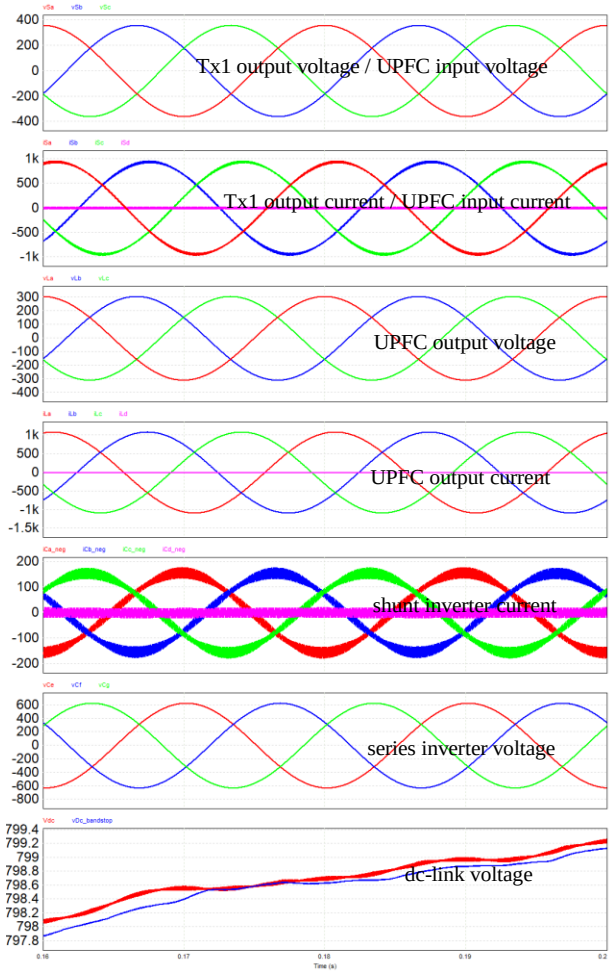


Figure B-7 Scenario 5 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-10 RMS measurements

	Phase A	Phase B	Phase C	Neutral
Input voltage	254	254	254	
Input current	663	663	663	8.6
Output voltage	217	217	217	
Output current	767	767	767	854
Shunt current	110	110	110	8.6
Series voltage	444	444	444	

Table B-11 Scenario 5 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
1. Source	168	162	0.96	168	162	0.96	168	162	0.96	505	485
2. Middle	195	189	0.972	195	189	0.972	195	189	0.972	585	569
3. Load	166	162	0.97	166	162	0.97	166	162	0.97	500	485
4. Shunt	28	-28	-1	28	-28	-1	28	-28	-1	84	-84
5. Series	28	-28	-1	28	-28	-1	28	-28	-1	85	-84
6. DC load											0

Figure B-7 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 5, and its RMS measurements are given in Table B-10. Table B-11 summarises the apparent power, real power and power factor of scenario 5.

In the scenarios 1 through 4, the input voltages are lower than the output voltages. Scenarios 5 through 8 are different that the input voltages are higher than the output voltages. This reversal of the voltage levels causes the power flow through the shunt and series inverters to be negative.

B.1.6 Scenario 6

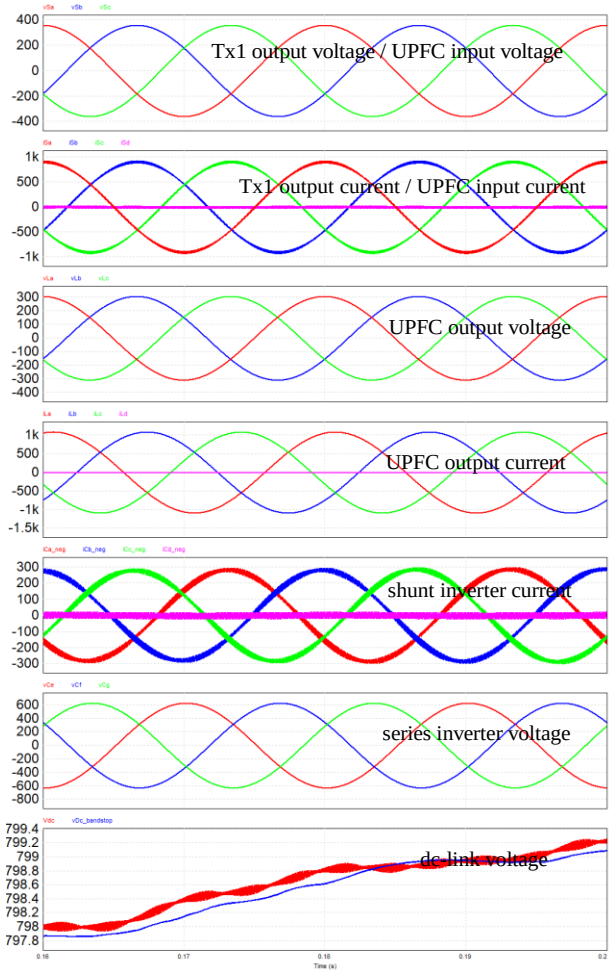


Figure B-8 Scenario 6 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-12 RMS measurements

	Phase A	Phase B	Phase C	Neutral
Input voltage	254	254	254	
Input current	638	638	638	9
Output voltage	217	217	217	
Output current	768	768	768	8.5
Shunt current	200	199	200	902
Series voltage	444	444	444	

Table B-13 Scenario 6 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
1. Source	162	162	1	162	162	1	162	162	1	485	485
2. Middle	195	190	0.972	195	190	0.972	195	190	0.972	585	569
3. Load	166	162	0.97	166	162	0.97	166	162	0.97	500	485
4. Shunt	51	-28	-0.55	50	-28	-0.55	50	-28	-0.55	151	-84
5. Series	28.4	-28	-0.98	28.4	-28	-0.98	28.4	-28	-0.98	85	-84
6. Dc load											0

Figure B-8 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 6, and its RMS measurements are given in Table B-12. Table B-13 summarises the apparent power, real power and power factor of scenario 6.

Scenario 6 is very similar to scenario 5. The only difference is that the target power factor seen by the transformer is changed from 0.97 to 1.0. The shunt inverter corrects the PF to be 1.0, in which increases its reactive power consumption. Other conditions remain similar.

B.1.7 Scenario 7

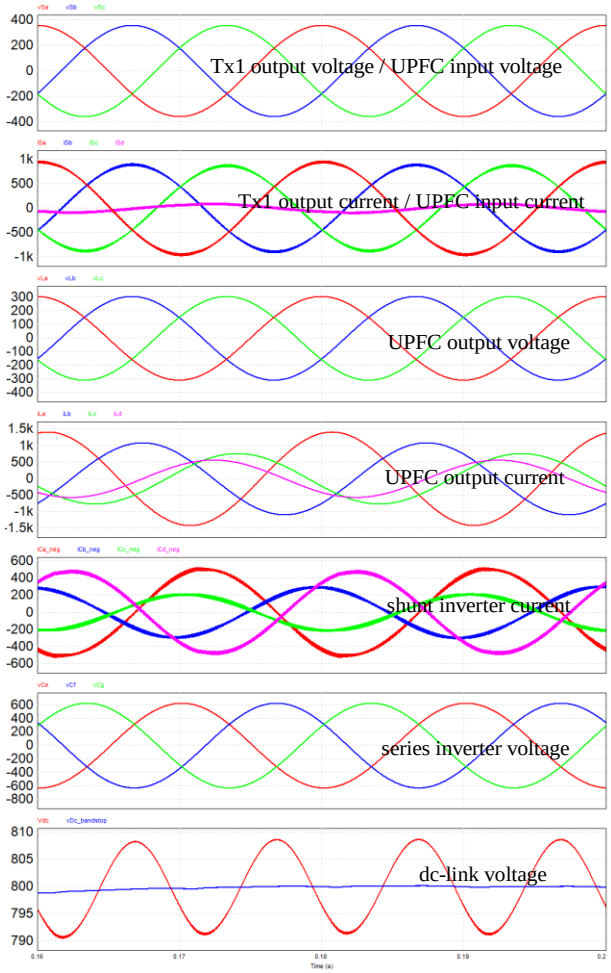


Figure B-9. Scenario 7 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-14. RMS measurements

	Phase A	Phase B	Phase C	Neutral
Input voltage	254	254	254	
Input current	672	672	672	62
Output voltage	217	217	217	
Output current	998	767	537	399
Shunt current	358	207	149	338
Series voltage	444	444	444	

Table B-15. Scenario 7 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
1. Source	170	170	1	159	159	1	156	156	1	485	485
2. Middle	253	246	0.972	195	189	0.972	136	132	0.972	585	569
3. Load	216	210	0.97	166	161	0.97	116	113	0.97	500	485
4. Shunt	91	-76	-0.94	52	-30	-0.58	37	23	0.61	181	-84
5. Series	37	-36	-0.98	28	-27	-0.98	20	-19	-0.98	85	-84
6. DC load											0

Figure B-9 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 7, and its RMS measurements are given in Table B-14. Table B-15 summarizes the apparent power, real power and power factor of scenario 7.

The change in scenario 7 from scenario 6 is the significant load imbalance, in which the phase A, B, and C are 130%, 100% and phase 70% of the average currents of all three phases. Due to the shunt inverter over current limits, the imbalance is only partially corrected by the shunt inverter, and the non-zero neutral current at the transformer terminal can be observed.

B.1.8 Scenario 8

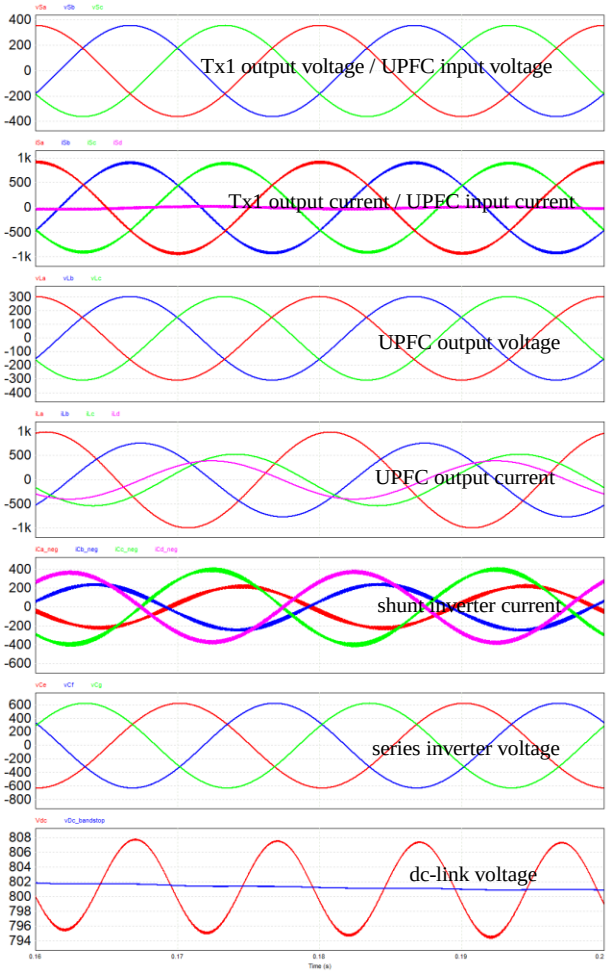


Figure B-10. Scenario 8 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-16. RMS measurements

	Phase A	Phase B	Phase C	Neutral
Input voltage	254	254	254	
Input current	652	643	634	20
Output voltage	217	217	217	
Output current	698	537	376	279
Shunt current	155	169	280	262
Series voltage	444	444	444	

Table B-17. Scenario 8 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
1. Source	165	165	1	163	163	1	160	160	1	489	489
2. Middle	177	172	0.972	136	132	0.972	95	93	0.972	409	398
3. Load	151	147	0.97	116	113	0.97	82	79	0.97	350	339
4. Shunt	39	-7	-0.18	43	30	0.71	71	67	0.95	152	91
5. Series	26	-25	-0.98	20	-19	-0.98	14	-14	-0.98	60	-58
6. Dc load											150

Figure B-10 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 9, and its RMS measurements are given in Table B-16. Table B-17 summarises the apparent power, real power and power factor of scenario 8.

The loads in scenario 8 is also imbalanced as is in scenario 7, but the ac load is reduced from 500kVA to 350kVA, and the dc port is loaded with 150kW. Due to the higher input voltages than the output voltages, an interesting condition is created that the dc load is supplied through by both the shunt and series inverters.

B.1.9 Scenario 9

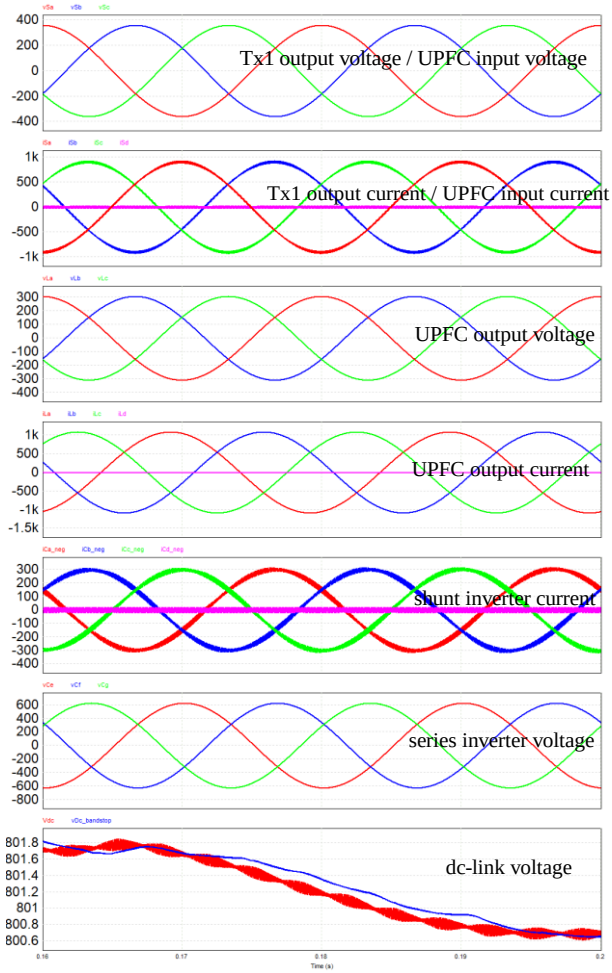


Figure B-11. Scenario 9 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-18. RMS measurements

	Phase A	Phase B	Phase C	Neutral
Input voltage	254	254	254	
Input current	636	636	636	8.9
Output voltage	217	217	217	
Output current	767	767	767	0
Shunt current	212	212	212	8.9
Series voltage	444	444	444	

Table B-19. Scenario 9 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
1. Source	162	-162	-1	162	-162	-1	162	-162	-1	486	-486
2. Middle	195	-189	-0.97	195	-189	-0.97	195	-189	-0.97	585	-566
3. Load	166	-161	-0.97	166	-161	-0.97	166	-161	-0.97	500	-484
4. Shunt	53.5	26.6	0.5	53.5	26.6	0.5	53.5	26.6	0.5	160	80
5. Series	28.4	27	0.95	28.4	27	0.95	28.4	27	0.95	85	81
6. DC load											0

Figure B-11 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 9, and its RMS measurements are given in Table B-18. Table B-19 summarises the apparent power, real power and power factor of scenario 9.

In the scenarios 9 through 11, the power flows from the load to the source side. The series inverter compensates the voltage difference between the source voltage and output voltage reference, and the shunt inverter supplies the power to the series inverter and corrects the power factor to be 1.0.

B.1.10 Scenario 10

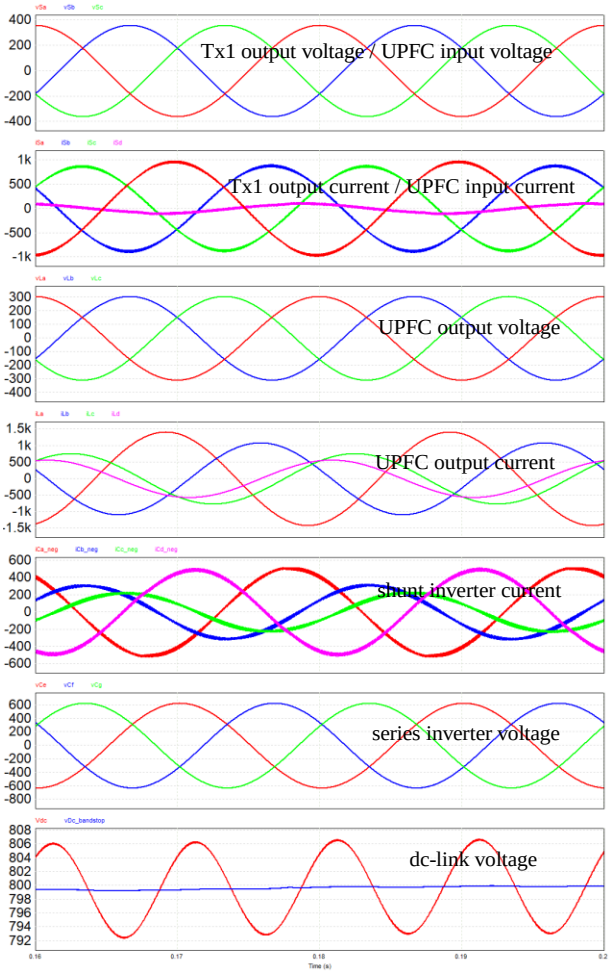


Figure B-12. Scenario 10 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-20. RMS measurements

	Phase A	Phase B	Phase C	Neutral
Input voltage	254	254	254	
Input current	676	620	610	70.5
Output voltage	217	217	217	
Output current	998	767	537	398
Shunt current	358	219	158	345
Series voltage	444	444	444	

Table B-21. Scenario 10 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
1. Source	172	172	-1	158	-158	-1	155	-155	-1	485	-485
2. Middle	253	-245	-0.97	195	-188	-0.97	136	-132	-0.97	585	-566
3. Load	216	-210	-0.97	166	-161	-0.97	116	-113	-0.97	500	-484
4. Shunt	91	73	0.81	55	30	0.55	40	-23	-0.58	186	80
5. Series	37	35	0.95	28	27	0.95	20	19	0.95	85	81
6. DC load											0

Figure B-12 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 10, and its RMS measurements are given in Table B-20. Table B-21 summarizes the apparent power, real power and power factor of scenario 10.

The change in scenario 10 from scenario 9 is the significant load imbalanced, in which the phase A, B, and C are 130%, 100% and phase 70% of the average currents of all three phases. Due to the shunt inverter over current limits, the imbalance is only partially corrected by the shunt inverter, and the non-zero neutral current at the transformer terminal can be observed.

B.1.11 Scenario 11

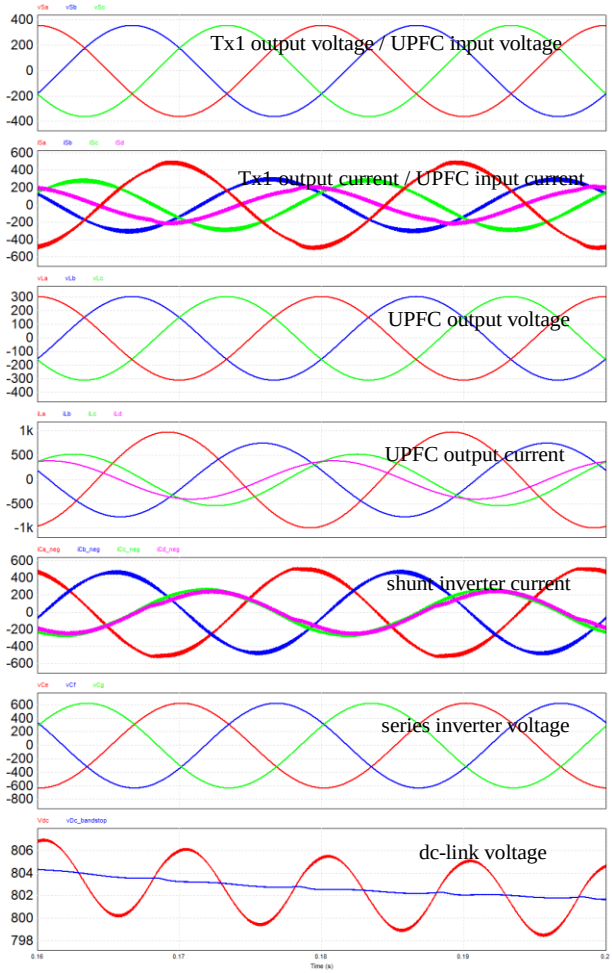


Figure B-13. Scenario 11 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-22. RMS measurements

	Phase A	Phase B	Phase C	Neutral
Input voltage	254	254	254	
Input current	339	210	199	141
Output voltage	217	217	217	
Output current	698	537	376	279
Shunt current	362	334	155	171
Series voltage	444	444	444	

Table B-23. Scenario 11 - Apparent power (kVA), real power (kW) and power factor

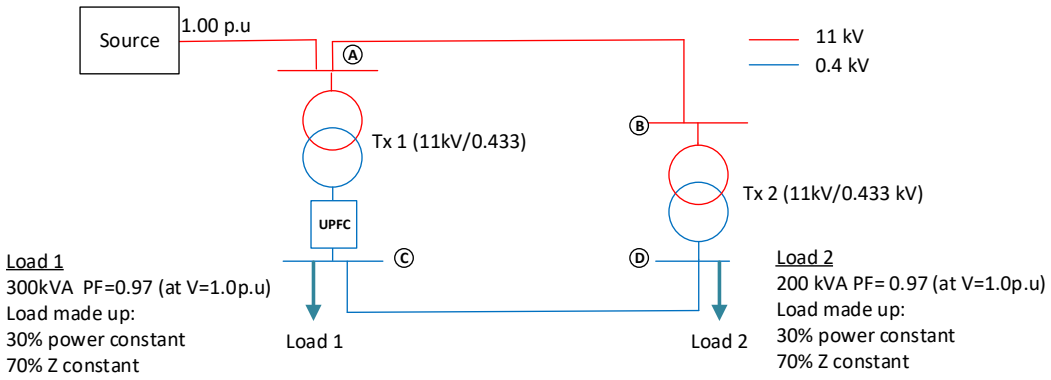
	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
1. Source	86	-85	-0.99	54	-53	-0.99	51	-50	-0.99	191	-190
2. Middle	177	-171	-0.97	136	-132	-0.97	95	-92	-0.97	409	-396
3. Load	151	-147	-0.97	116	-113	-0.97	816	-79	-0.97	350	-339
4. Shunt	92	86	0.93	84	78	0.92	47	41	0.88	224	206
5. Series	26	25	0.95	20	19	0.95	14	13	0.95	60	57
6. DC load											151

Figure B-13 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 11, and its RMS measurements are given in Table B-22. Table B-23 summarises the apparent power, real power and power factor of scenario 11.

The loads in scenario 11 is also imbalanced as is in scenario 10, but the ac load is reduced from 500kVA to 350kVA, and the dc port is loaded with 150kW. Due to the shunt inverter over current limits, the imbalance is only partially corrected by the shunt inverter, and the non-zero neutral current at the transformer terminal can be observed.

B.2 Mesh Network Scenarios Provided by SPEN

Table B-24 is a summary of the Mesh Network test scenarios considered for simulation and analysis. EGB used PSIM simulation package to model and simulate the UPFC operation under these conditions, the results are provided in the body of this section.



		R (Ohm)	X (Ohm)
Source	A	0.4695	0.054462
A	B	0.4695	0.054462
C	D	0.044914	0.011158

Figure B-14. Network configuration for various Mesh scenarios for demonstration of SST Topology 1 (UPFC)

Table B-24. Mesh scenario cases

Scenario	Imbalance (Load 1 and Load 2)	P & Q target (power seen by Tx1)	Target imbalance
1	0%	300kVA Pf=0.97	0%
2	0%	300kVA Pf=1	0%
3	0%	0.0 kVA	0%
4	0%	500kVA pf=0.97	0%
5	30%	300kVA Pf=0.97	0%
6	30%	300kVA Pf=1	0%
7	30%	0.0 kVA	0%
8	30%	500kVA pf=0.97	0%

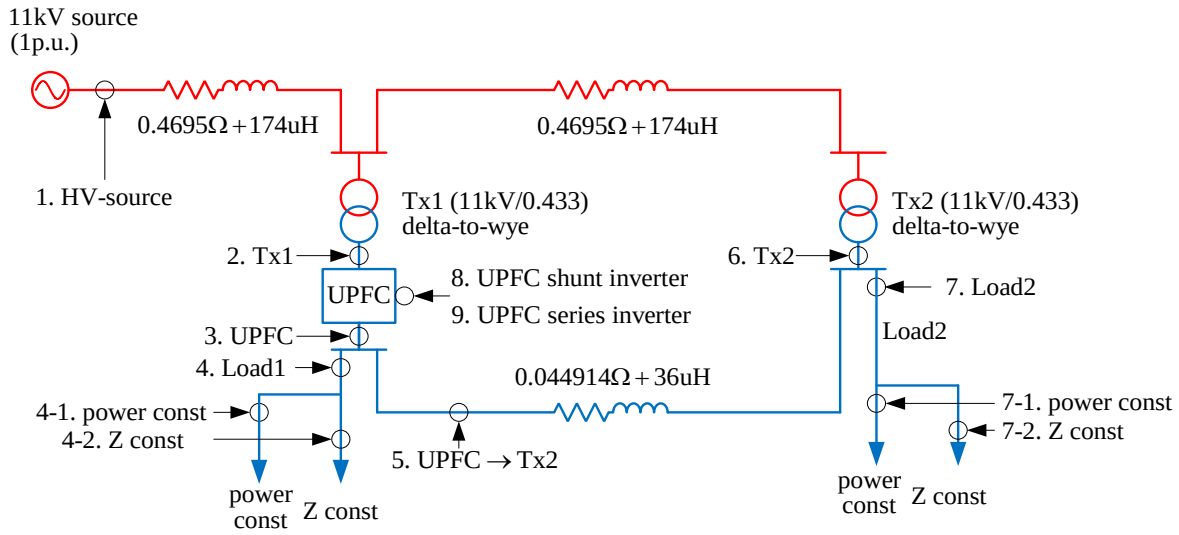


Figure B-15. Network configuration for various Mesh scenarios with power measurement points (Redrawn)

Table B-25. Load 1 and 2 conditions for scenarios

	case 1,2,3,4		case 5,6,7,8	
	Load 1	Load 2	Load 1	Load 2
Load (kVA)	300	200	300	200
Imbalance	0%	0%	30%	30%
power constant load (Total) (kVA)	90	60	90	60
RMS line-to-neutral 1 p.u. phase voltage (V) 400V/sqrt(3)	230.9			
phase A power (kVA)	30	20	39	26
phase B power (kVA)	30	20	30	20
phase C power (kVA)	30	20	21	14
Z constant total load (kVA)	210	140	210	140
phase A power (kVA)	70	46.667	91	60.667
phase B power (kVA)	70	46.667	70	46.667
phase C power (kVA)	70	46.667	49	32.667
Phase A - L load (H)	5.896E-04	8.844E-04	4.535E-04	6.803E-04
phase A - R load (Ohm)	7.390E-01	1.109E+00	5.685E-01	8.527E-01
Phase B - L load (H)	5.896E-04	8.844E-04	5.896E-04	8.844E-04
phase B - R load (Ohm)	7.390E-01	1.109E+00	7.390E-01	1.109E+00
Phase C - L load (H)	5.896E-04	8.844E-04	8.423E-04	1.263E-03
phase C - R load (Ohm)	7.390E-01	1.109E+00	1.056E+00	1.584E+00
phase A power (kVA)	100	66.667	130	86.667
phase B power (kVA)	100	66.667	100	66.667
phase C power (kVA)	100	66.667	70	46.667

Figure B-14 illustrates the network configuration for various Mesh scenarios, Table B-24 list the Mesh scenario cases, which are given by Ali (SPEN). Figure B-14 is redrawn as Figure B-15 to include the

line impedances and power measurement points. Total of nine points are selected as the measurements points as follows.

1. High voltage (HV) source power
2. Low voltage (LV) Transformer 1 (Tx1) output power
3. UPFC output power
4. Load 1 power (4-1. Power const. load and 4-2. Z const. load)
5. UPFC to transformer 2 (Tx2) power through the Mesh mode
6. LV-Tx2 output power
7. Load 2 power (7-1. Power const. load and 7-2. Z const. load)
8. UPFC shunt inverter
9. UPFC series inverter

Also, the Load 1 and Load 2 conditions are given in Table B-25 based on Table B-24 and 1 p.u. RMS line-to-line voltage at 400V (i.e. RMS line-to-neutral at 230.9V).

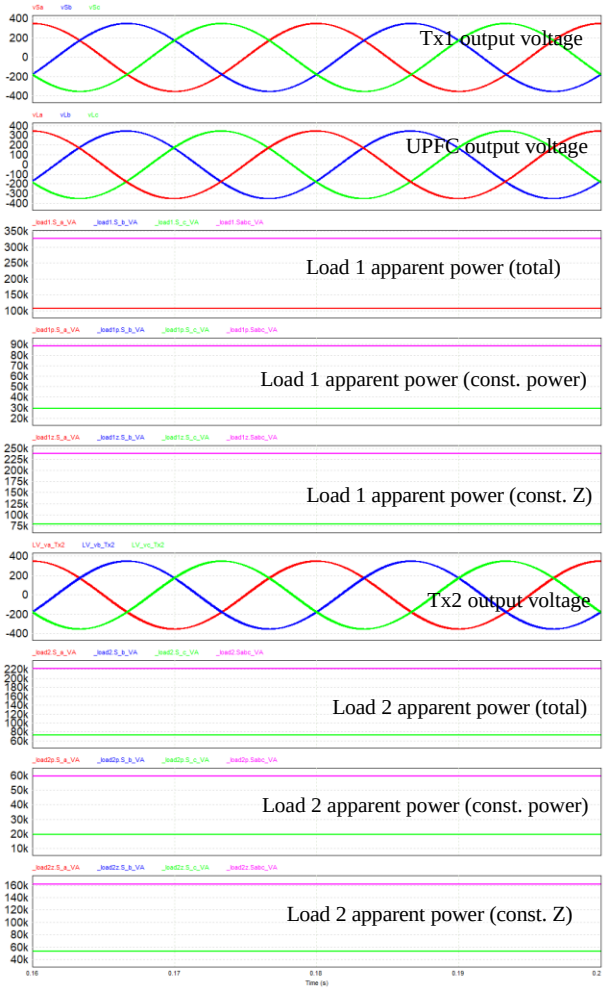


Figure B-16. Tx1, Tx2, and UPFC output voltage and Load 1 and 2 powers

Table B-26. Tx1, Tx2, and UPFC output voltage and Load 1 and 2 powers

Tx1 output voltage	249V rms
Tx2 output voltage	249V rms
UPFC output voltage	247V rms
Load 1 apparent power (total power)	328 kVA (target 300kVA)
Load 1 apparent power (const. power)	89 kVA (target 90kVA)
Load 1 apparent power (const. Z)	239 kVA (target 210 kVA)
Load 2 apparent power (total power)	222kVA (target 200 kVA)
Load 2 apparent power (const. power)	60 kVA (60kVA)
Load 3 apparent power (const. Z)	162 kVA (140kVA)

Figure B-16 illustrates and

Table B-26 lists the Tx1, Tx2, and UPFC output voltage and Load 1 and 2 powers of scenario 1. The transformer's voltage conversion ratio assumes 11kV at primary and 0.433 kV at secondary. Furthermore, the simulation assumes that the Tx1 and Tx2 are ideal without any losses; therefore, the output voltages of Tx1, Tx2, and UPFC are RMS line-to-neutral voltage approximately at 249V, 249V, and 247V, respectively, which are greater than 1 p.u. voltage at 230.9V. This leads to higher power loads from the constant impedance loads, and in turn, it causes to higher power loads than the target power load conditions. The constant power load meets the target power loads. This phenomenon applies to most scenarios, but the terminal voltages are lower than 1 p.u. in some scenarios, and then, the power load is lower than the target power load conditions.

B.2.1 Scenario 1

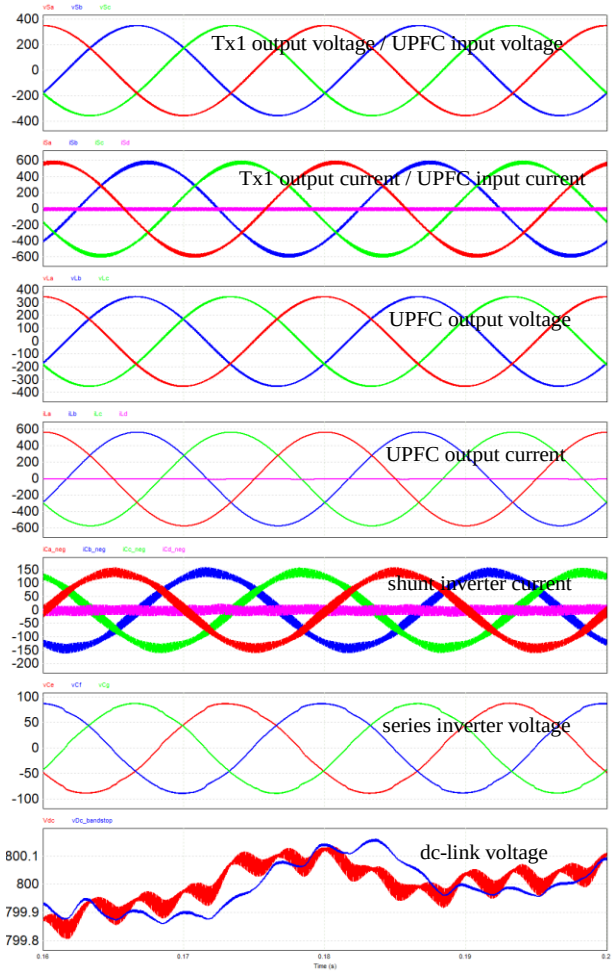


Figure B-17. Scenario 1 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-27. Scenario 1 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
HV-source	192	179	0.934	192	179	0.934	192	179	0.934	576	537
Tx1	102	99	0.97	102	99	0.97	102	99	0.97	306	296
UPFC	99	99	1	99	99	1	99	99	1	297	296
Load1	109	106	0.97	109	106	0.97	109	106	0.97	328	317
UPFC→Tx 2	26	-7	-0.27	26	-7	-0.27	26	-7	-0.27	79	-21
Tx2	91	79	0.88	91	79	0.88	91	79	0.88	272	238
Load2	74	72	0.97	74	72	0.97	74	72	0.97	222	216
shunt inv.	25	-1.2	-0.05	25	-1.2	-0.05	25	-1.2	-0.05	75	-3.6
series inv.	2	-1.1	-0.53	2	-1.1	-0.53	2	-1.1	-0.53	6	-3.3

Figure B-17 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 1. Table B-27 summarizes the apparent power, real power and power factor of scenario 1.

The series inverter of the UPFC is assigned to control the UPFC's output PF and output power, in which their control targets are set to be PF = 1 and 300kVA/kW. Due to this setting, the UPFC only processes 300kW from the load 1, and in turn, all the reactive power and any active power over 300kW from load 1 is loading the Tx2. This causes the PF of Tx2 to be at 0.87 despite the PF of the load 2 is only 0.97. Additionally, the scenario calls for the PF at Tx1 to 0.97; therefore, all the reactive power of the shunt inverter is creating the PF of 0.97 at the Tx1 when the UPFC output PF is 1. The real power flow through the shunt and series inverters are small.

B.2.2 Scenario 2

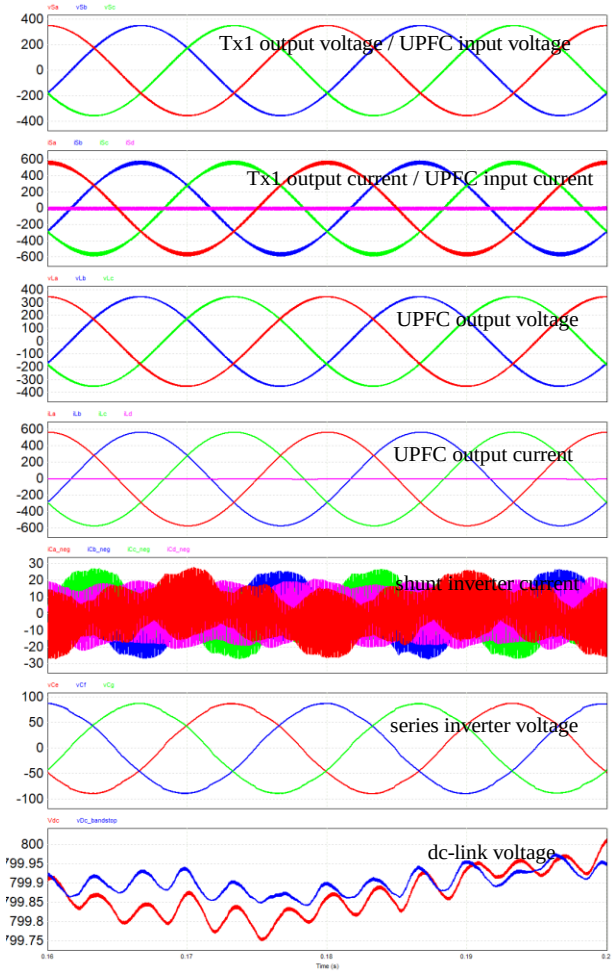


Figure B-18. Scenario 2 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-28 Scenario 2 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
HV-source	184	179	0.972	184	179	0.972	184	179	0.972	553	537
Tx1	99	99	1	99	99	1	99	99	1	296	296
UPFC	99	99	1	99	99	1	99	99	1	296	296
Load1	109	106	0.97	109	106	0.97	109	106	0.97	328	318
UPFC→Tx2	26	-7	-0.27	26	-7	-0.27	26	-7	-0.27	78	-21
Tx2	91	79	0.88	91	79	0.88	91	79	0.88	272	238
Load2	74	72	0.97	74	72	0.97	74	72	0.97	222	216
shunt inv.	1.2	-1.2	-1	1.2	-1.2	-1	1.2	-1.2	-1	3.6	-3.6
series inv.	2	-1.1	-0.54	2	-1.1	-0.54	2	-1.1	-0.54	6	-3.3

Figure B-18 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 2. Table B-28 summarizes the apparent power, real power and power factor of scenario 2. Scenario 2 is very similar to scenario 1, and only different is that the PF at Tx1 is changed from 0.97 to 1. Because of this, all the reactive power processed by the shunt inverter is nearly zero. Other conditions remains the same.

B.2.3 Scenario 3

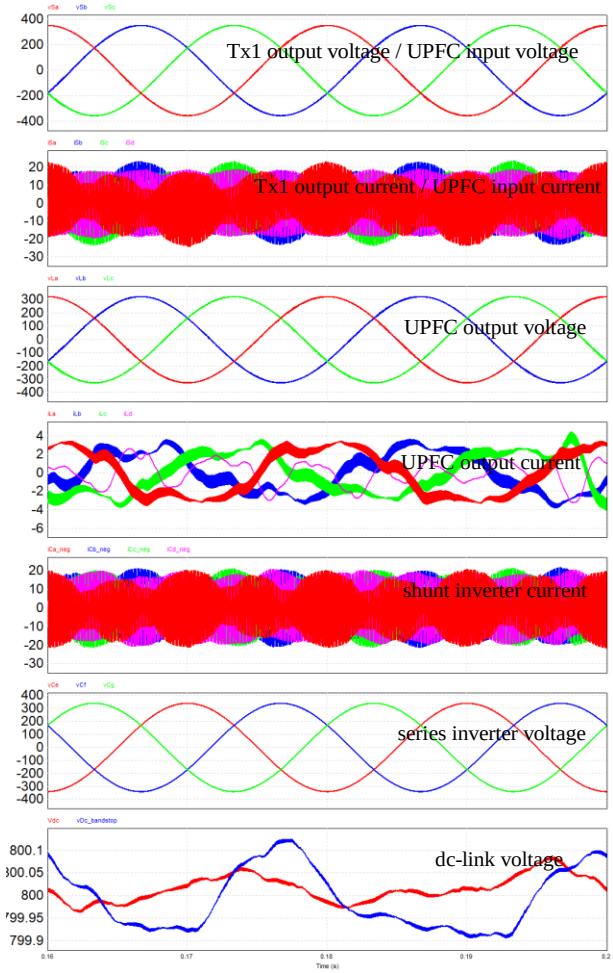


Figure B-19. Scenario 3 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-29 Scenario 3 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
HV-source	179	174	0.97	179	174	0.97	179	174	0.97	539	523
Tx1	3.1	0.3	1	3.1	0.3	1	3.1	0.3	1	9.3	0.9
UPFC	0.5	0.5	0.97	0.4	0.4	0.96	0.4	0.4	0.96	1.3	1.3
Load1	96	94	0.97	96	94	0.97	96	94	0.97	289	281
UPFC→Tx2	96	-93	-.97	96	-93	-.97	96	-93	-.97	288	-280
Tx2	178	173	0.97	178	173	0.97	178	173	0.97	535	519
Load2	74	72	0.97	74	72	0.97	74	72	0.97	222	215
shunt inv.	0.2	-0.2	-0.8	0.2	-0.2	-0.7	0.2	-0.1	-0.7	0.7	-0.5
series inv.	0.04	-.04	-1	0.04	-.04	-1	0.04	-.04	-1	0.12	-.12

Figure B-19 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 3. Table B-29 summarizes the apparent power, real power and power factor of scenario 3. The series inverter of the UPFC is assigned to control the UPFC's output power to be zero. Due to this setting, all the power from the load 1 and load 2 are processed by the Tx2. The output voltages of Tx1, Tx2, and UPFC are RMS line-to-neutral voltage approximately at 249V, 249V, and 229V. The total power of the load 1 is lower than 300kVA because the UPFC output voltage is lower than 1 p.u.

B.2.4 Scenario 4

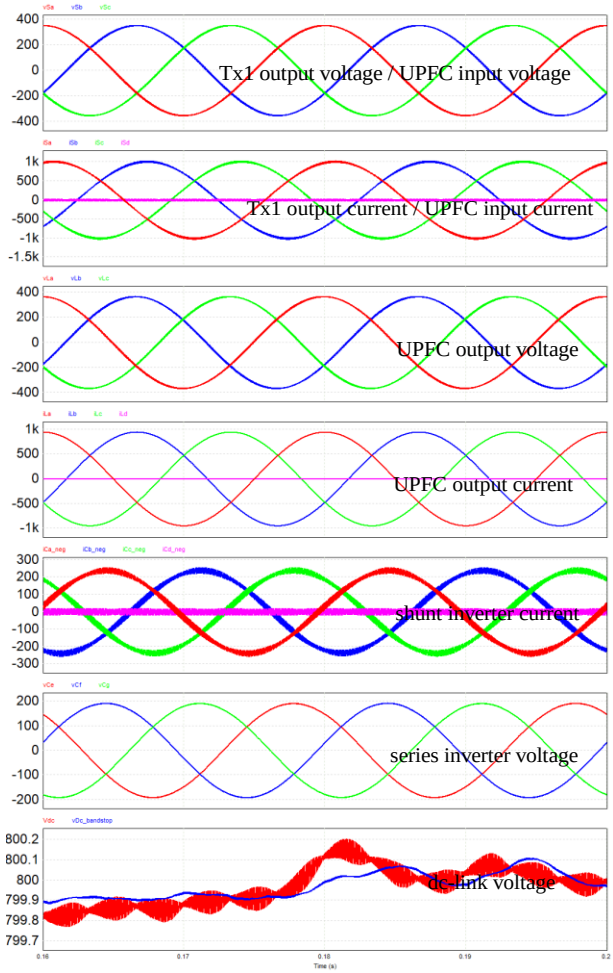


Figure B-20. Scenario 4 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-30 Scenario 4 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
HV-source	208	190	0.912	208	190	0.912	208	190	0.912	625	570
Tx1	177	172	0.97	177	172	0.97	177	172	0.97	531	516
UPFC	172	172	1	172	172	1	172	172	1	517	516
Load1	118	115	0.97	118	115	0.97	118	115	0.97	355	344
UPFC→Tx2	63	58	0.92	63	58	0.92	63	58	0.92	188	172
Tx2	47	17	0.36	47	17	0.36	47	17	0.36	140	51
Load2	74	72	0.97	74	72	0.97	74	72	0.97	223	216
shunt inv.	42	5.7	0.13	42	5.7	0.13	42	5.7	0.13	125	17
series inv.	7.5	5.8	0.77	7.5	5.8	0.77	7.5	5.8	0.77	23	17

Figure B-20 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 4. Table B-30 summarizes the apparent power, real power and power factor of scenario 4.

The series inverter of the UPFC is assigned to control the UPFC's output PF and output power, in which their control targets are set to be PF = 1 and 500kVA/kW. Due to this setting, the UPFC processes and

supply 516kW of real power. There is some power error of about 16kW, and its reason is being debugged. Since the UPFC only processes real power from the load 1 and load 2, all the reactive power is pushed to the Tx2, which yields its PF to be about 0.36.

Like scenario 1, scenario 4 calls for the PF at Tx1 to 0.97; therefore, all the reactive power of the shunt inverter is creating the PF of 0.97 at the Tx1 when the UPFC output PF is 1. The real power flow through the shunt and series inverters are relatively small.

B.2.5 Scenario 5

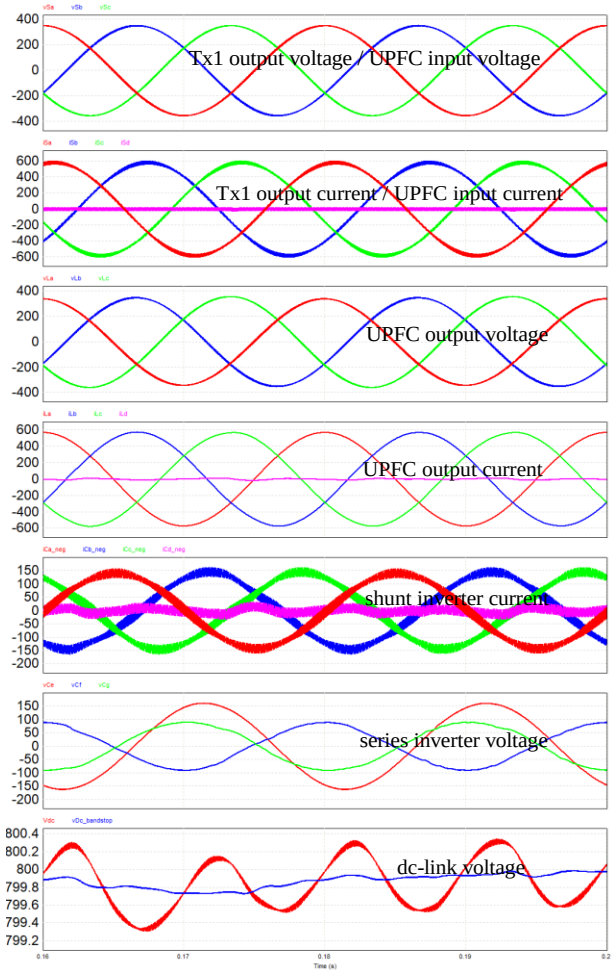


Figure B-21. Scenario 5 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table 31 Scenario 5 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
HV-source	216	208	0.961	198	171	0.867	163	156	0.957	578	536
Tx1	102	99	0.97	102	99	0.97	102	99	0.97	306	296
UPFC	97	96.6	1	99	99	1	101	101	1	297	297
Load1	136	132	0.97	109	106	0.97	80	77	0.97	325	315
UPFC→Tx2	48	-35	-0.74	26	-7	-0.27	30	24	0.79	104	-18
Tx2	142	131	0.92	91	80	0.88	41	27	0.66	274	237
Load2	96	93.4	0.97	74	72	0.97	52	50.4	0.97	222	216
shunt inv.	25	-1.3	-0.53	25	-1.2	-0.48	25	-1.1	-0.24	75	-3.6
series inv.	3.8	-3.4	-0.89	2.1	-1.1	-0.53	2.2	1.2	0.59	8.1	-3.2

Figure B-21 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 5. Table B-31 summarizes the apparent power, real power and power factor of scenario 5. The series inverter of the UPFC is assigned to control the UPFC's output PF and output power, in which their control targets are set to be PF = 1 and 300kVA/kW. Also, the series inverter output amplitudes and phases are adjusted, as shown in Figure B-21 series inverter voltage, to create a balanced UPFC output power despite the loads are unbalanced.

Similar to scenarios 1 and 4, scenario 5 calls for the PF at Tx1 to 0.97; therefore, all the reactive power of the shunt inverter is creating the PF of 0.97 at the Tx1 when the UPFC output PF is 1. The real power flow through the shunt and series inverters are relatively small.

B.2.6 Scenario 6

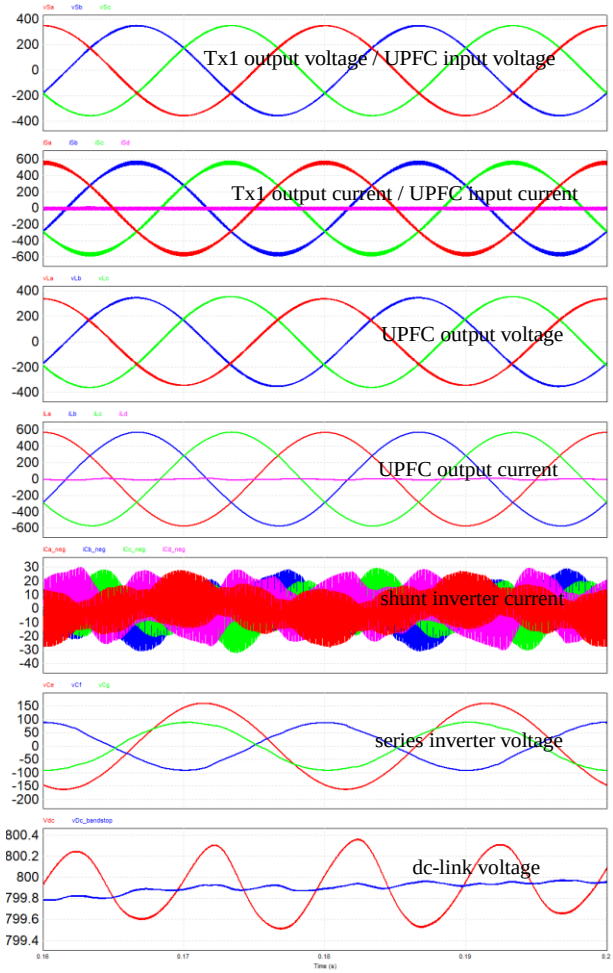


Figure B-22. Scenario 6 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-32 Scenario 6 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
HV-source	211	208	0.98	186	182	0.92	157	156	0.99	556	536
Tx1	99	99	1	99	99	1	99	99	1	296	296
UPFC	97	97	1	99	99	1	101	101	1	296	296
Load1	136	132	0.97	109	106	0.97	80	77	0.97	326	315
UPFC→Tx2	48	-35	-.74	26	-7	-.27	30	24	0.8	103	-18
Tx2	142	131	0.92	90.6	76	0.88	41	27	0.66	274	237
Load2	96	93	0.97	74	72	0.97	52	50	0.97	222	216
shunt inv.	1.32	-1.3	-1	1.22	-1.2	-1	1.03	-1	-1	3.6	-.36
series inv.	3.8	-3.4	-0.9	2.1	-1.1	-.53	2.2	1.2	0.59	8.1	-3.3

Figure B-22 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 6. Table B-32 summarizes the apparent power, real power and power factor of scenario 6. Scenario 6 is very similar to scenario 5, and only different is that the PF at Tx1 is changed from 0.97 to 1. Because of this, all the reactive power processed by the shunt inverter is nearly zero. Other conditions remain the same.

B.2.7 Scenario 7

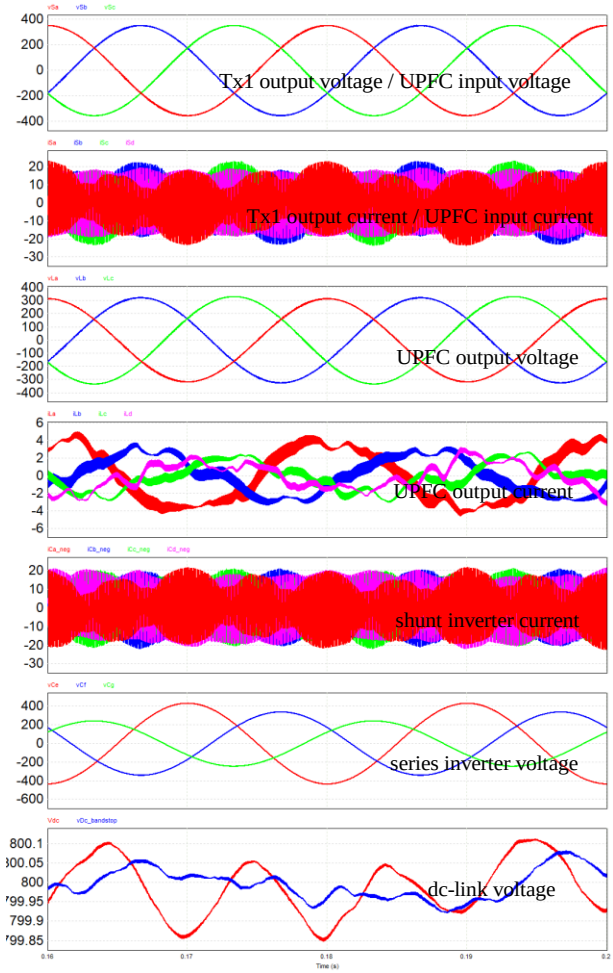


Figure B-23. Scenario 7 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-33 Scenario 7 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
HV-source	205	202	0.985	182	167	0.917	154	152	0.99	542	522
Tx1	0.3	0.3	1	0.3	0.3	1	0.3	0.6	1	0.9	0.9
UPFC	0.6	0.6	0.97	0.44	0.4	0.96	0.3	0.3	0.95	1.37	1.3
Load1	120	117	0.97	96	94	0.97	70	68	0.97	287	278
UPFC→Tx2	120	-116	-0.97	96	-93	0.97	70	-68	-.97	286	-277
Tx2	229	222	0.97	178	173	0.97	126	122	0.97	534	518
Load2	96	93	0.97	74	72	0.97	52	50	0.97	222	215
shunt inv.	0.4	-0.4	-0.87	0.2	-.15	-0.72	1.1	0	-.66	0.72	-0.5
series inv.	0.07	-.07	-0.96	0.03	-.04	-0.96	0.02	-.02	-.95	0.13	-.12

Figure B-23 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 7. Table B-33 summarizes the apparent power, real power and power factor of scenario 7. The series inverter of the UPFC is assigned to control the UPFC's output power to be zero, in which the series inverter output amplitudes and phases are adjusted, as shown in Figure B-23's series inverter voltage, to create a zero UPFC output power despite the loads are unbalanced.

B.2.8 Scenario 8

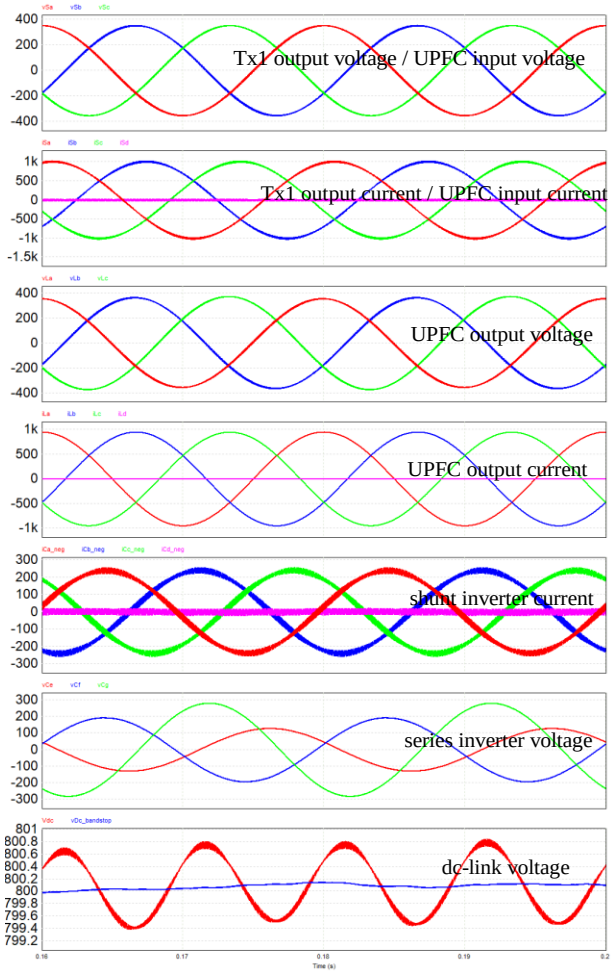


Figure B-24. Scenario 8 - UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage

Table B-34 Scenario 8 - Apparent power (kVA), real power (kW) and power factor

	Phase A (kVA, kW)			Phase B (kVA, kW)			Phase C (kVA, kW)			Total (kVA, kW)	
	S	P	PF	S	P	PF	S	P	PF	S	P
HV-source	232	219	0.945	216	182	0.844	178	166	0.934	627	569
Tx1	177	172	0.97	177	172	0.97	177	172	0.97	531	516
UPFC	168	168	1	172	172	1	176	176	1	516	516
Load1	147	142	0.97	118	114	0.97	86	84	0.97	352	341
UPFC→Tx2	41	25	0.62	63	57	0.92	94	92	0.98	197	175
Tx2	89	69	0.78	47	17	0.36	48	-3.6	-0.76	183	50
Load2	96	93	0.97	74	72	0.97	52	50	0.97	222	216
shunt inv.	42	5.6	0.13	42	5.6	0.13	42	5.9	0.14	126	17.3
series inv.	5	1.8	0.36	7.6	5.8	0.76	11	9.9	0.89	23.7	17.6

Figure B-24 illustrates the UPFC input and output voltage and current, shunt inverter current, series inverter voltage, and dc-link voltage of scenario 8. Table B-34 summarizes the apparent power, real power and power factor of scenario 8.

The series inverter of the UPFC is assigned to control the UPFC's output PF and output power, in which their control targets are set to be PF = 1 and 500kVA/kW. The series inverter output amplitudes and phases are adjusted, as shown in Figure B-'s series inverter voltage, to create a balanced UPFC output

power despite the loads are unbalanced. Since the UPFC only processes real power from the load 1 and load 2, all the reactive power is pushed to the Tx2, which yields its PF to be much less than 0.97. In a particular case of Tx2 Phase C, the power flow is negative.

B.3 Detection of interconnected and radial network

It is possible that the transition from interconnected network to radial (and vice versus) may not be reported to the SST in a real-time.

illustrates the NOP status communication window. A control signal will alert the SST of a NOP status change between OPEN and CLOSE. During this time frame, LV-SST does not know the precise moment of NOP status change. Furthermore, the NOP status may change asynchronously to each other.

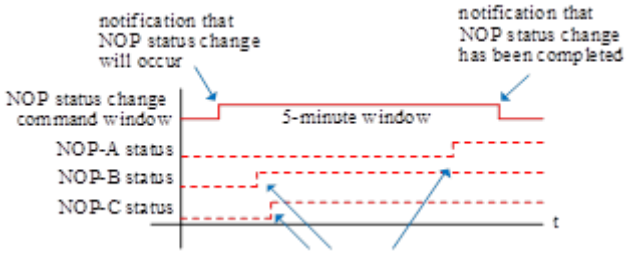


Figure B-25 NOP status communication window

Figure B-25 illustrates the NOP status detection simulation results. A passive detection method is utilized to detect the NOP transition from closed to open (i.e. Mesh to Radial transition). During Mesh mode, the inverter is grid-following (i.e. the output voltage is held stiff by the grid). Therefore, as soon as the NOP opens and the connection to the grid is lost, one or combination of output voltage amplitude, phase, frequency, harmonics, etc. goes out of specification. When this deviation is detected, the controller can switch over from the current control (Mesh mode) to the voltage control (Radial mode).

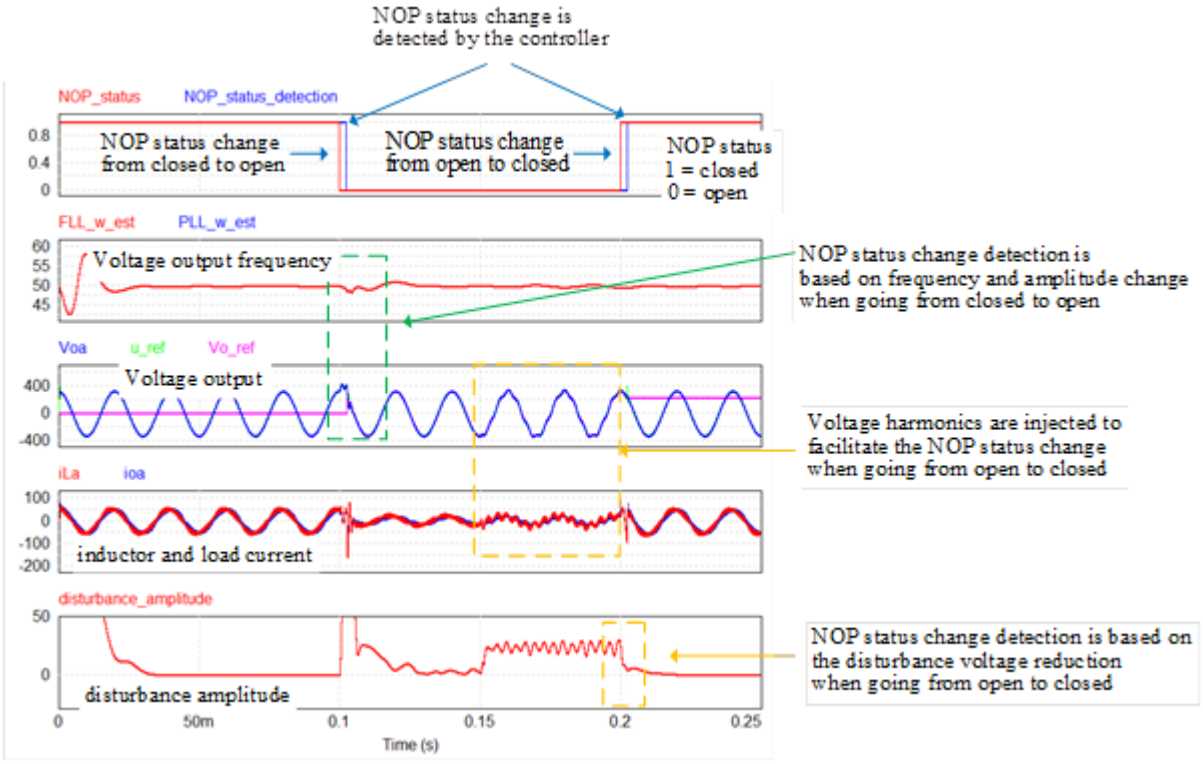
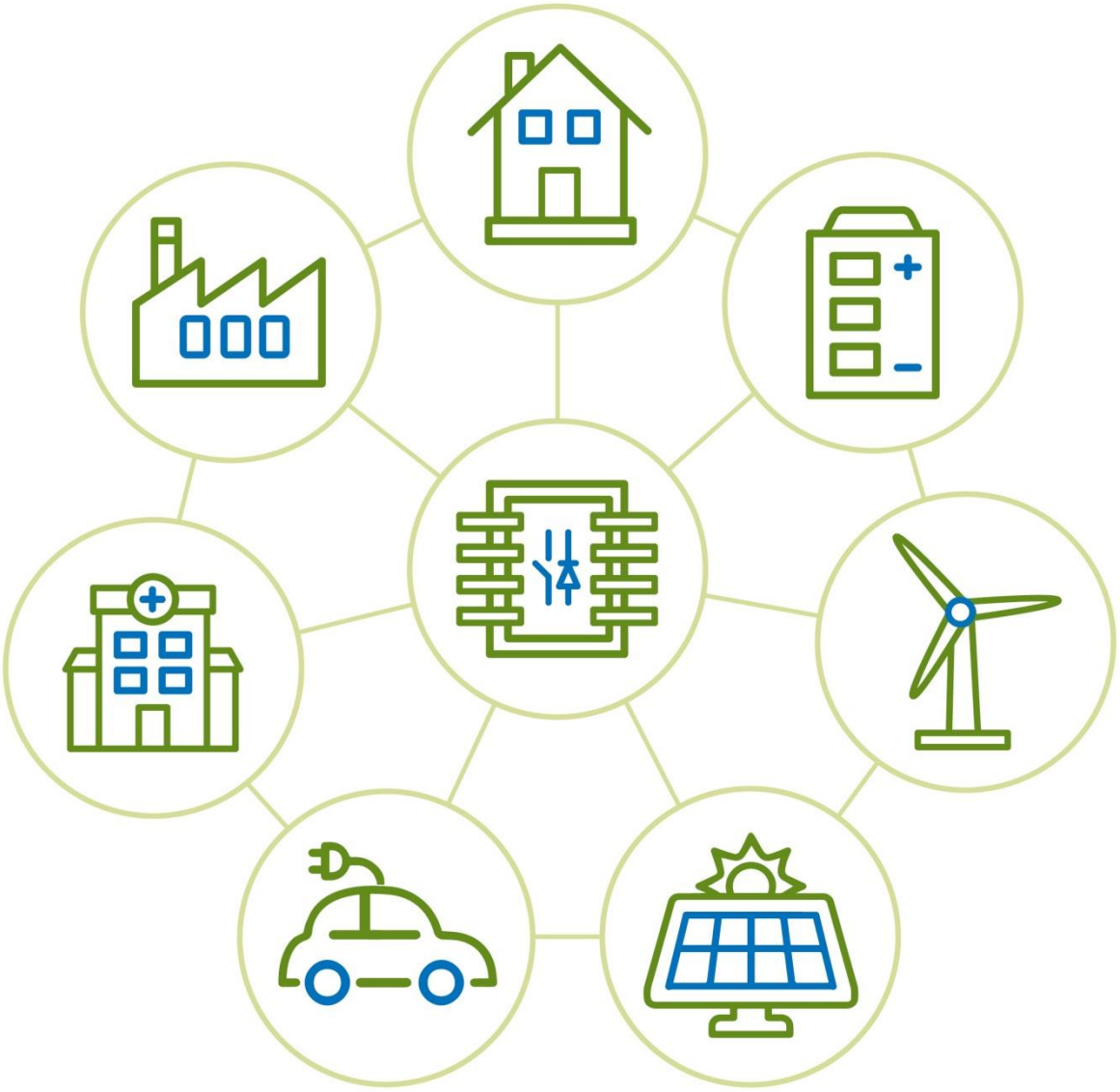


Figure B-26 NOP status detection simulation results

Different detection methods are required to detect the NOP transition from open to closed (i.e. Radial to Mesh transition). During Radial mode, the inverter is grid-forming (i.e. the output voltage is controlled by the inverter). A passive NOP detection may not work during this transition because it is difficult to distinguish between a normal load change and the load change due to a NOP closing during the voltage control mode. An active voltage injection method has been proposed. Before the NOP is closed, a high frequency harmonic signals are injected to the output voltage, and the injected high frequency voltage is monitored. When the NOP closes, the stiff grid voltage over-rides the high frequency voltages, and the detection is completed when the monitored high frequency voltage amplitude is reduced below a threshold.



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