SP ENERGY NETWORKS

LV ENGINE

Smart Transformer Hardware, Power Converter Control and Reliability

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Contents

Glossary of Terms

Abbreviation	Definition
AC	Alternating Current
ADC	Analog to Digital Conversion
Al	Aluminium
B2B	Back-to-Back
CC	Current Control
CHB	Cascaded H-Bridge
CSPI	Cooling System Performance Index
DAB	Dual Active Bridge
DBC	Direct Bonded Copper
DC	Direct Current
DPC	Direct Power Control
DSL	Digital Subscriber Line
DSOGI	Dual Second Order Generalized Integration
DSP	Digital Signal Processors
dsrfPLL	Decouple Double Synchronous Reference Frame PLL
EMI	Electromagnetic Interface
EMIF	External Memory Interface
ESR	Equivalent Series Resistance
FDP	Failure Distribution Function
FIFO	First-In-First-Out
FLL	Frequency Locked Loop
FPD	Frequency Phase Detector
FPGA	Field Programmable Gate Array
GaN	Galium Nitride
HT	Hybrid Transformer
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
LASJ	Large Area Solder Joint
LF	Loop Filter
LFT	Line-Frequency Transformer
LV	Low Voltage
MAC	Multiple Active Bridge
MLCC	Multilayer Ceramic Capacitor
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPPF	Metallized Polypropylene Film
MV	Medium Voltage
NOP	Normal open point
NPC	Neutral Point Clamped
OCT	Onload Tap Changer
PCI	Peripheral Component Interconnected
PD	Phase Detector
PI	Proportional Integral
PLC	Power Line Communication
PLL	Phase Locked Loop
PoF	Physics of Failure
PR	Proportional Resonant
PV	Photovoltaic
PWM	Pulse Width Modulation
Q	Reactive power
QSG	Quadrature Signal Generator

RMS	Root Means Square
Si	Silicon
SiC	Silicon Carbide
SOGI	Second Order Generalized Integration
SPWM	Sinusoidal Pulse Width Modulation
SRC	Series Resonance Converter
SRF	Synchronous Reference Frame
SST	Solid State Transformer
ST	Smart Transformer
STATCOM	Static Synchronous Compensator
THD	Total Harmonic Distortion
TR	Transformer
uPP	Universal Parallel Port
VC	Voltage Control
VCO	Voltage Controller Oscillator
VOC	Voltage Oriented Control
VSC	Voltage Source Converter
WBG	Wide Band Gap

Executive Summary

This report builds on the previous academic works and also a fresh literature review to identify key hardware, software and reliability requirements for a Smart Transformer (ST). The findings of this report, where they are deemed to be appropriate, will be used for development of Smart Transformer technical specification and also informing the product design as part of LV Engine project. SP Energy Networks (SPEN) is delivering LV Engine project funded by Ofgem which aims to install Smart Transformers within power distribution secondary substations (11/0.4kV) with the goal to provide voltage control capability, active/reactive power control capability and dc-connectivity. For the tendering of the ST, this report provides key recommendations, which are mandatory for the ST to provide the desired functionality in the different trial sides.

The report is separated in three subsections, which are addressing the following contents:

(1) **Hardware for the ST:** Review of potential ST designs by means of their power converter architectures, topologies, power semiconductor technology, the required devices and definition of hardware requirements
(2) **Software for the ST:** Review of software by means of controller design and communication for the power electronics of the ST
(3) **Reliability for the ST:** Review on reliability challenges and reliability requirements for the ST

In the following, the main contents are separated by the subsections and the main findings are summarized. The first subsection, addressing the **hardware for the ST**, includes the following contents and findings:

- The On Load Tap Changer (OLTC) and hybrid transformer are discussed as potential alternatives to the ST. A qualitative comparison with the ST is made in terms of functionality, power density, reliability, efficiency and costs.
- A comprehensive review on ST architectures is provided and the architectures are grouped in dependence of the number of power stages (single-stage, two-stages, and three-stages) and the modularity level (non-modular, semi-modular and modular). The characteristics of each configuration are investigated with respective advantages and disadvantages in terms of independent control of MV and LV grid, harmonic filtering capability and DC connectivity.
- The architectures are grouped in dependence of the number of power conversion stages and the modularity. The applicability of the architectures in the LV Engine schemes is evaluated by means of the capability to provide grid services, such as DC connectivity, power flow control, harmonic filtering and reactive power control.
- The hardware costs of different topologies are qualitatively estimated by consideration of the number of power semiconductors, filter requirements and software design effort.
- The selection of major components (power semiconductor technology, cooling system and medium frequency transformer) and its impact on the system is examined. For the power semiconductor technology, the advantages and disadvantages of wide band gap devices are elaborated and compared with Si-devices in terms of efficiency, switching frequency, robustness, technology maturity and costs. Furthermore, the impact of each technology on the different power stages is evaluated and recommendations for the application of suitable technology for each power conversion stage are made. For the cooling system, the characteristics of air-cooling and liquid-cooling systems are presented and compared in

terms of cooling system performance. For the medium frequency transformer, the core materials are examined as well as the impact of the dielectric stress for the transformer.

- The costs and efficiency of LV and MV side converters are estimated by benchmarking commercial power converters: PV converters for the LV side and commercially available MV converters for MV side. Furthermore, for the DC/DC stage in the three-stage configuration, the impact of the number of building blocks on the costs and the efficiency is discussed. The results provide criteria for the specification of the ST requirements.
- The sizing of the power semiconductors is analysed for the different operation modes of the ST and the permitted disturbances for which the ST has to stay grid-connected. The design requirements for the power semiconductors in terms of their voltage and current ratings is provided. Additionally, the impact of fuses in the feeders and the required fault current is discussed.

The section addressing **software for the ST** contains the following contents and findings:

- Control requirements for each power stage considering different ST architectures (single-stage, two-stage and three-stage configurations) are addressed. The control objective of the LV side converter is determined in accordance with the LV Engine schemes.
- The ST controller design in different reference frames (stationary and rotating) is discussed. Furthermore, the two required control modes (grid forming and grid feeding) are examined. As a resulting challenge, the transition between the two control modes is highlighted and a solution is proposed.
- The grid synchronization is addressed and the importance to select a suitable algorithm is highlighted. Various Phase Locke Loop (PLL) schemes are reviewed and their control performance (static and dynamic) is compared.
- The capability to connect DC-grids to the ST is examined, showing possible architectures with either DC/DC or AC/DC converters. Here, the considered DC-grid features a bipolar LVDC (±750 V) grid.
- The implementation of the control algorithm is addressed from the control hardware point of view, considering DSPs and FPGAs. The features of each device are presented and a hybrid solution is described considering the communication interfaces between them.
- The features of the centralized control, decentralized control and multi-agent based control are considered and the implementation of different control loops in different centralized/decentralized units is recommended.
- Possible communication interfaces of a ST-fed grid are addressed considering the date rate and the communication distance.

The section addressing the **reliability of the ST** contains the following contents and findings:

- Reliability and availability definition along with a discussion about the use of a constant failure rate for reliability evaluation
- Analysis of the impact of a fault on the system operation in the different LV-engine schemes.
- Identification of the expected most sensitive components of the ST, which are power semiconductors, capacitors and the cooling system. Root causes for their failure are examined.
- Innovative concepts for the increase of reliability for the most sensitive components are described and the temperature is identified as a critical stressor for multiple components.

- Challenges for the humidity and the condensation in the substation of the ST are described and the impact on the components of the ST are examined.
- Operation and maintenance concepts for the ST are discussed and a report from the applications in wind turbines is used to provide recommendations to achieve high reliability.

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1. Introduction to the LV Engine project

1.1. Background

SP Energy Networks initiated the LV Engine project with the goal to support the transition to a low carbon economy in Great Britain [1]. The key objective of the project is to design and trail the deployment of Smart Transformers (ST)s in the distribution grid within secondary substations (11/0.4kV) for ensuring a sufficient hosting capacity of the electrical network for renewable energy sources and electric vehicle charging stations. In contrast to the conventional transformer, which is a passive device, the ST enables to provide voltage control, power flow control and dc-grid connectivity. The employment of the ST will be trailed in five LV Engine schemes, whereas three of them address the installation in a pure AC-grid and the other two target the connection of DC-grids.

The installation of Smart Transformers in the electrical distribution grid requires interdisciplinary cooperation in the fields of power system, power electronics and communications. With respect to medium voltage connectivity and potentially employed medium frequency transformers, there is a lack of industrial products and designs need to be evaluated carefully, whether they can provide the desired functionalities. Moreover, the interaction of power electronics with the grid and its protection results in an interaction, which needs to be considered during the design procedure. Thereby, the interaction between hardware and software also impacts the resulting requirements for the rating of the hardware.

Power converters are commonly applied for the grid-connection in renewable energy sources or Static Synchronous Compensators (STATCOM)s. However, in the LV Engine project, the power electronics need to act in voltage control mode (for radial networks) and in power control model (for meshed networks), which challenges the control and the communication of the ST. Moreover, the reliability of the ST is of major importance to provide a high quality of service to the customers in the distribution grid. Therefore, the reliability of the ST requires to be set to very high standards already in the design and redundancy needs to be considered to increase the reliability.

This technical report investigates suitable hardware for the ST, software for the ST and reliability challenges for the ST. It concludes recommendations for the design of the ST.

1.2. Report scope and objectives

The goal of this report is to support the tendering for the ST hardware and software specifications within the scope of the LV Engine project. In additions, it is the goal to inform potential manufactures about possible design solutions. This includes:

- Understanding which power converters are suitable in the scope of the LV Engine schemes and which ones will not be capable to fulfil the specifications of the projects
- Analyse different components and technologies for the ST and to evaluate their impact on the functionality and the performance of the ST
- Analyse the required control and communication, which is required to provide the desired functionality of the ST
- Identify challenges in the controller design and the communication of the ST
- Identify reliability challenges and provide potential solutions to overcome them

For meeting these objectives, a comprehensive literature review is made and solutions for ST applications and an evaluation is performed. Moreover, solutions from other power electronics applications are selected and those solutions are considered for ST applications.

1.3. Report structure

The report is structured as follows:

- Section 2 addresses the hardware of the ST
- Section 3 addresses the software of the ST
- Section 4 addresses the reliability of the ST
- Section 5 identifies key findings and recommendations
- Section 6 provides conclusions.

2. Hardware for the Smart Transformer

2.1. From line-frequency transformer to the Smart Transformer

In the following subsection, a short introduction to the ST is provided. The conventional transformer and potential other solutions for increasing the controllability in the grid are introduced and their potential functionality is described.

The conventional Line-frequency Transformer (LFT) is the key element of electrical distribution grids. It provides galvanic isolation and adapts voltage levels for energy transmission. However, it is a passive element and does not provide any controllability, which is desired in certain conditions. To enable voltage adaption of the LFT, the Onload Tap Changer (OTC) has been developed and enables changing the voltage with discrete step sizes. However, to the current state, the dynamics of the OTC are very limited and the phase angle between input voltage and output voltage is fixed.

For extending the controllability, the Hybrid Transformer (HT) has been proposed [2, 3]. The HT is a combination of LFT with a power converter, which has been proposed to enhance the limited functionalities of the LFT with an OTC. Technically, this approach exploits the inherent characteristic of the power converters, which facilitates the control of different electrical parameters and therefore ancillary grid services. The potential configurations of HTs are briefly described in the following.

Hybrid Transformer in shunt configuration

The power converter for AC-DC conversion is connected in parallel with the LFT as shown in **Figure 1**, which is the so-called Static Synchronous Compensator (STATCOM). It enables to inject reactive current into the grid and therefore the grid voltage and the power factor can be controlled. The functionality of active filtering to eliminate harmonics in the grid can be provided.

Hybrid Transformer in series configuration (Field upgradeable transformer) [4]

As shown in **Figure 2**, the power converter can be connected in series on the low voltage side or the medium voltage side. Therefore, it enables manipulating the grid voltage and the power factor. Similar to the shunt configuration, it can act as an active harmonic filter.

(a) (b)

Figure 1: Hybrid Transformer in shunt configuration: (a) Magnetic coupling and (b) Direct coupling.

Figure 2: Hybrid Transformer in series configuration: (a) Magnetic coupling and (b) Direct coupling.

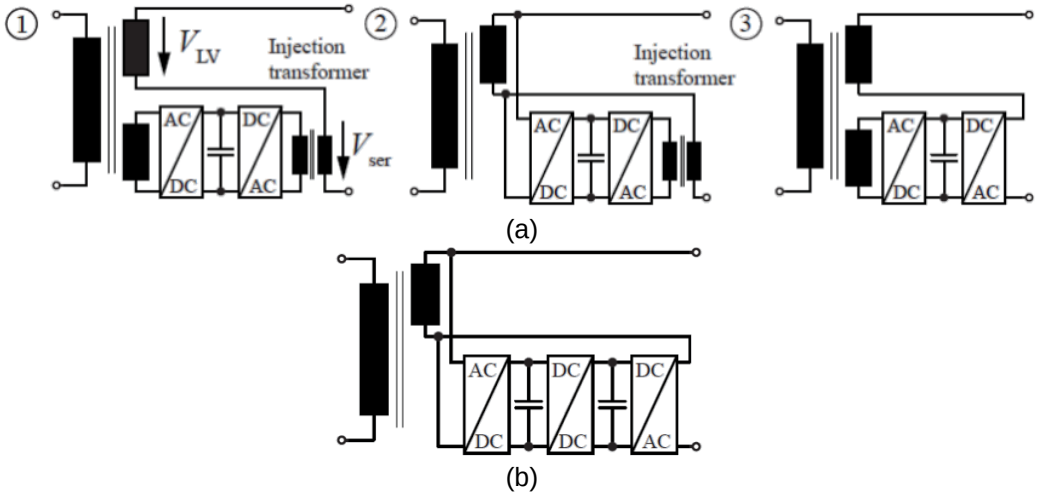


Figure 3: Combined configuration: (a) Magnetic coupling and (b) Direct coupling.

Hybrid Transformer in shunt and series configuration [5]

The combined configuration consists of a shunt and a series configuration, which is connected to the same DC-link as a back-to-back converter. The configurations are shown in **Figure 3**.

Unlike the configurations presented before, active and reactive voltage/current can be supported by the power converter.

Concept of the Smart Transformer

In traction application, the potential volume and weight reduction have encouraged developments for the substitution of the LFT with a medium frequency transformer fed by power semiconductors. The resulting system is referred to as Solid State Transformer (SST). The SST is transferring the overall power, which differentiates it from the HT. In the SST application, the volume and weight reduction are the main driver of the technology. However, the SST in Smart grid applications is not motivated by the volume and weight, but the control and communication capability, which makes the SST smart and therefore, it is referred to as Smart Transformer (ST). It is a series element in the grid and enables decoupling of the connected AC grids to a certain extent. In grid forming operation, the ST is able to control the grid voltage and the grid frequency – independently from the other AC and DC grids potentially connected to the ST.

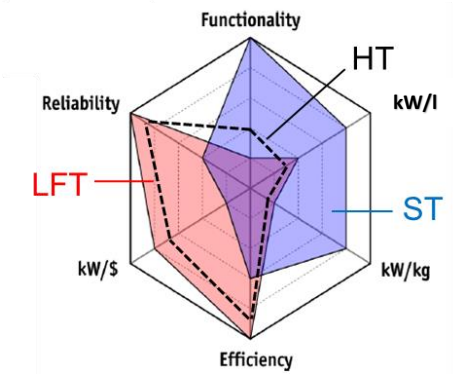


Figure 4: Comparison of LFT, HT and ST performance characteristics.

Comparison of Hybrid Transformer, low frequency transformer and Smart Transformer

The HT concept enables to enhance the controllability of the LFT with the partly rated power converter. The ST instead is solution for replacing the LFT and providing full controllability of the grid, whereas it needs to be rated for the full power. The controllability and the rated power of the HT are typically 10-20% with respect to the rating of the ST [6]. Apart from the controllability, the performance in terms of weight, volume, costs and efficiency is essential and needs to be considered. As an extension of [6], the four characteristics are compared for the ST, the LFT and the HT in **Figure 4**. Here, it should be noted that only material cost is considered, implying that a labour costs, software and profits are not taken into account. In the weight and volume calculation, DC-link capacitors, power semiconductors, heatsink, filter inductors, transformer, electronics and cabinet/frame are considered. For the evaluation of the losses, the filter inductors and power semiconductors are considered. The ST has a significantly lower volume in comparison to the LFT, whereas the material cost and losses are increased to 460 % and 280 %, respectively [6]. The major contribution to the weight and volume of the ST are the passive filter components. Hence, the filter design is of particular interest. The emerging technologies such as Silicon Carbide (SiC) can be used to realize the higher switching frequency and consequently enable reducing volume and weight of the passive components. In addition, the efficiency can be improved by using wide band gap devices with their lower losses.

2.2. ST architectures classification

Several power converter architectures with applicability to the ST have been proposed in literature. In the following they are grouped in order to provide the fundamentals for their comparison. As pointed out before, the ST is encouraged by the capability to provide grid services. These grid services are strongly correlated to the number of DC links and power conversation stages. Therefore, the ST architectures are grouped in dependence of the number of power conversion stages as shown in **Figure 5:** the single stage for direct conversion between MVAC-LVAC, two stages for MVAC-LVDC-LVAC and three stages for MVAC-MVDC-LVDC-LVAC. A representation of the architectures is shown in **Figure 6**. In the following, the advantages and disadvantages are discussed.

As a requirement for the system, a storage element, such as a DC link, is essential for decoupling the connected grids of the ST. With the availability of the storage element, the converter architecture may provide the following features:

- Independent generation of the voltage in the grid (MV and LV)
- Harmonic filtering capability
- DC- connectivity for DC-links (e.g. for EV charging stations or battery storage)

Single stage configuration:

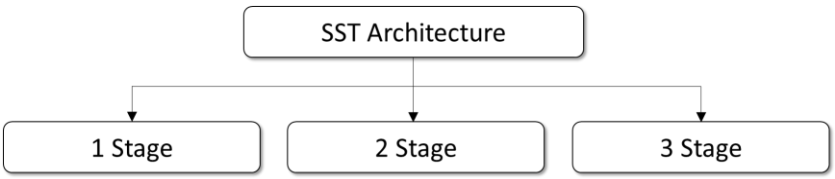


Figure 5: ST architecture classification in dependence of the number of power stage.

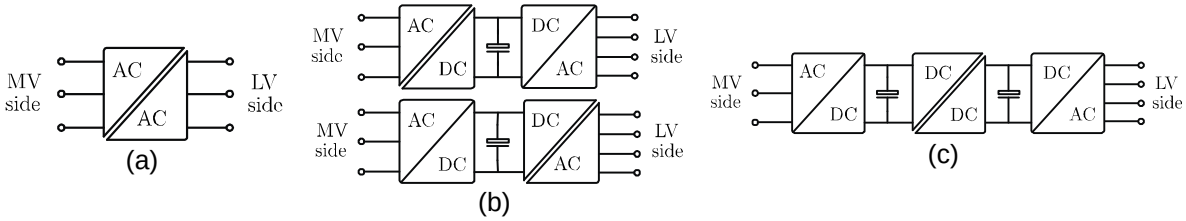


Figure 6: Example of (a) 1 stage, (b) 2 stages and (c) 3 stages configurations.

The single power stage concept (as shown in **Figure 6 (a)**) is based on the direct power conversion between MVAC and LVAC, providing galvanic isolation. This can be achieved with matrix converter topologies, which do not require bulky DC-link capacitors. In addition, with only a single power conversion stage, the configuration of the whole system can be simple and a low number of power semiconductors is required. For the single stage ST architectures, not even DC-link capacitors are required. Consequently, the single power conversion stage may result in high power density at low cost. However, due to the lack of DC-links the MV and LV grids are strongly coupled by the energy flow, similar to the conventional line-frequency transformer. Therefore, a disturbance on one side of the grid will also be seen on the other side of the grid. An independent control of the grid voltage in the MV and LV grid is not possible. This is of high importance if services are provided and the ST needs to inject reactive power in one side of the grid or compensate current harmonics/voltage harmonics in the grid. Automatically, the other grid will be affected and potentially see a higher distortion. Therefore, matrix converters are not practical to provide grid services, because of the strong coupling of the grids.

Two stages configuration:

Two-stages ST architectures (as shown in **Figure 6 (b)**) can be designed with a high flexibility and in literature voltage source converter based architectures, current source converter based architectures and a mixture of both architectures have been proposed. Voltage source converter based architectures use capacitors for energy storage, whereas current source converters use inductors for the storage of energy. Both enable to provide services and to not have limitations with respect to their applicability in the LV Engine schemes. However, voltage source converters are mostly used in commercial products. Potential reasons for the preference of voltage source converter are doubts about the performance of current source converters (e.g. losses and common mode voltages) and the security in case of emergency shut down. As an additional objection for current source converters, power semiconductors with inverse voltage blocking capability are required.

In the two stages architecture with voltage source converters, the galvanic isolation is implemented either in the MV- or the LV-side. Depending on the implementation of the isolation stage, one of DC-link is available (i.e. with the MV-side galvanic isolation the LVDC grid is provided, whereas the MVDC is available when the LV-side is adopting the galvanic isolation) [7]. Depending on the adopted topology for the two stages, the grid services may be limited. However, with one DC-link in the system, the grids can be decoupled and services can be provided for most of the architectures.

As a point to consider carefully, the galvanic isolation may be provided by a medium frequency transformer or a low frequency transformer. In the latter case, there will not be the benefit in terms of weight and volume reduction of the ST.

A current source converter based architecture with two power conversion stages and no DC-links has been also proposed [8]. The drawbacks of currents source converters have been already highlighted.

Three stages configuration:

The three-stage ST architectures (as shown in **Figure 6 (c)**) are based on the galvanic isolation by means of the MVDC to LVDC stage, which provides certain flexibly to adopt topologies for each stage. Hence, there is a possibility to provide both MVDC and LVDC connectivity and the MVAC

and LVAC grids can be decoupled [9]. Furthermore, all grid services such as reactive power

compensation, bidirectional power flow, renewable energy and energy storage system integration, can be provided. However, a higher number of power semiconductors and capacitors are needed for this architecture and therefore the costs for the system may be higher - despite the use of devices rated for low voltage.

As a second level of classification, the 3 stages configuration is divided into three categories as shown in **Figure 7**: non-modular, semi-modular and modular. For each of these concepts, an example for the isolation stage is shown in **Figure 8**.

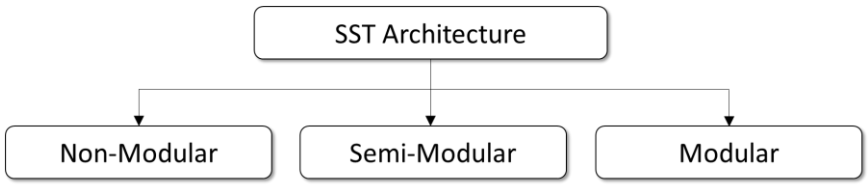


Figure 7: ST architecture classification in accordance with the modularity.

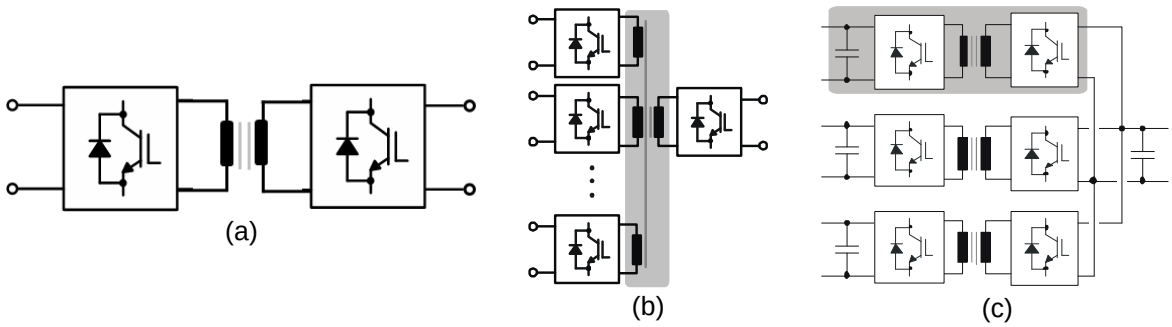


Figure 8: Example of (a) non-modular, (b) semi-modular (shown only DC-DC stage) and (c) modular concept (shown only DC-DC stage).

Non-modular:

Non-modular architectures require a lower number of power devices, but a high voltage blocking capability of power devices for the MV-side. Unfortunately, for Si-based devices high switching losses are associated with high blocking voltages and to our best knowledge devices with a sufficient high blocking voltage for the ST application are not commercially available at this point (IGBTs for blocking voltages higher than 6.5 kV). Furthermore, big output filters are required, fault

tolerance schemes are not available and scalability in power and voltage is not possible. As an example for this topology, the single-phase Dual Active Bridge (DAB) is shown in **Figure 8 (a)**.

Semi-modular:

The semi-modular concept is only applicable in the converter stage in which the isolation is realised, because it holds a transformer with multiple windings. This is not present in the other converter stages. Multi-winding medium/high frequency transformers are used for a single cell, which enables to reduce the number of transformers. In the application with high input/output voltage ratio, it enables to use devices rated for lower voltage, because several power converter cells are connected to a same transformer. As an example, the multi-winding structure is shown in **Figure 8 (b)**.

Modular:

The modularity concept is based on the use of several building blocks, which are connected in parallel and/or in series. Modular power converters commonly enable to adopt fault tolerant schemes and scalability in power/voltage. Because of the modularity, a higher number of components, such as transformer cores and power devices is needed. As an example for modular DC/DC converters, several series-input-parallel-output connected dual active bridges are shown in **Figure 8 (c**).

2.3. ST topologies for the different power conversion stages

In this section, typical building blocks for power converters in a three stages ST are presented. First, typical converter structures for the stages of a three stages architecture are presented. Remarkably, the medium voltage stage topology and the isolation stage are coupled in many architectures, whereas the low voltage stage can be chosen independently.

For the MV stage converter, multi-level topologies are usually chosen, because of the potential advantages of optimizing the design trade-offs in consideration of:

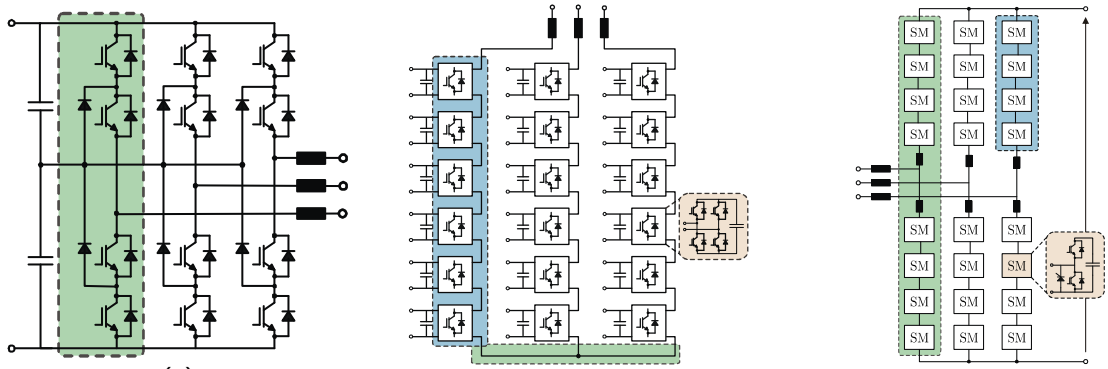


Figure 9: Example for MV stage converter in the 3 stages configuration; (a) Neutral Point Clamped (NPC), (b) Cascaded H-Bridge (CHB) and (c) Modular Multilevel Converter (MMC).

1) reduced dv/dt (EMI noises),
2) reduced filter size,
3) higher efficiency,
4) lower blocking voltage of power devices.

The multi-level topologies as an example are shown in **Figure 9**, where Neutral Point Clamped (NPC) in **Figure 9 (a)**, Cascaded H-bridge (CHB) in **Figure 9 (b)** and Modular Multilevel Converter (MMC) in **Figure 9 (c)**.

The galvanic isolation is essentially required in the isolation stage, where a medium/high frequency transformer is used. Hence, the size/weight of the passive components can be reduced, compared with the transformer designed for the line-frequency. Moreover, a higher efficiency can be achieved by reducing the switching losses with soft-switching power converter topologies. The Series Resonance Converter (SRC) as shown in **Figure 10 (a)** does not require a closed loop control, but the input and output ports are strongly coupled. This means a disturbance in one DC-link directly affect the other DC-link, even if a certain dynamic behaviour needs to be considered. The DAB, shown in **Figure 10 (b)**, and the Multiple Active Bridge (MAB), shown in **Figure 10 (c)**, need to be controlled instead. Therefore, both ports can be decoupled, whereby the MAB is consisting of a single multi-winding transformer. Consequently, the number of the passive components is reduced at the expense of losing some part of advantages of the modular concept. The number of reduced components is associated with the number of H-Bridges adopted in the LV-side of the MAB. In this topology, the multi-winding transformer is of high importance and it its failure interrupts the operation of all connected H-bridges. Therefore, it is recommended to select a sufficiently low number of H-Bridges.

Considering the development of the efficiency of high frequency transformers, the DAB topology is taken as an example. Its trend of increasing efficiency is shown in Table ***1***, where three references from literature are compared. As it can be seen, the efficiency has been increasing up to maximum 98.8 % with Wide BandGap (WBG) devices of SiC-MOSFET and the core material of

FINEMET for the transformer. Furthermore, the use of WBG devices operated with a higher switching frequency enables the use of smaller passive components.

For the LV stage converter, a 4-wire configuration is employed and connected in parallel for high current capability. Similar to the MV side converter, the multi-level topologies, which are shown in **Figure 11 (b)** and **(c)** are beneficial for reducing dv/dt and passive components with a higher efficiency, although the 2-level topology in **Figure 11 (a)** is well known and established.

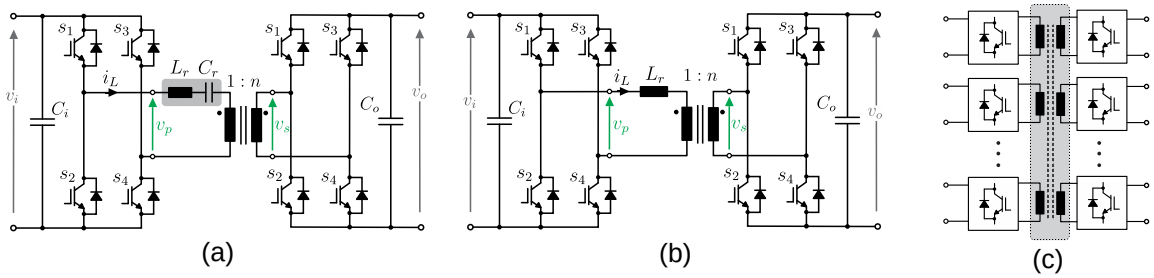


Figure 10: Example for DC/DC stage converter in the 3 stages configuration; (a) Series Resonance Converter (SRC), (b) Dual Active Bridge (DAB) and (c) Multiple Active Bridge (MAB).

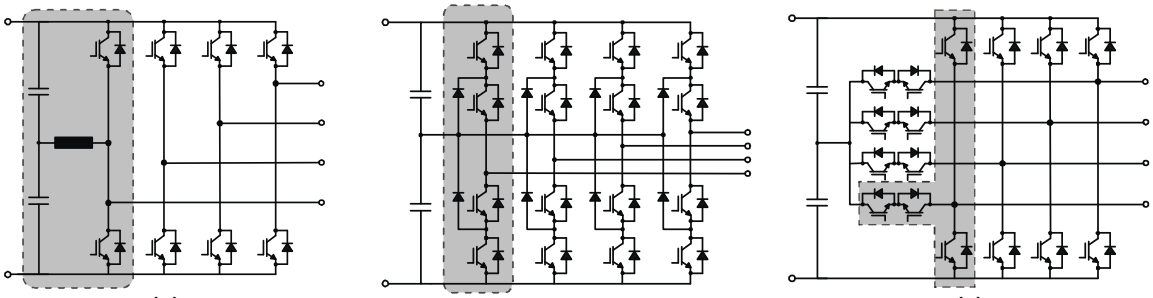


Figure 11: Example for LV stage converter in the 3 stages configuration; (a) 2-Level, (b) NPC and (c) T-type 4-wire Voltage Source Inverter (VSI).

Table 1: Development of the efficiency for DAB converters over time.

Year	1992 (by M.H.Kheraluwala)	2007 (by S. Inoue)	2016 (by H.Akagi)
Power device	Plannar-Gate Si-IGBT	Trench-Gate Si-IGBT	Trench-Gate SiC-MOSFET
Rated power @ fsw	50 kW @ 50 kHz	10 kW @ 20 kHz	100 kW @ 20 kHz
Medium/high frequency transformer	Ferrite	FINEMET	FINEMET
Efficiency @ power	<90%	96.8 % @ 10 kW 97.4 % @ 3.8 kW	98 % @ 100 kW 98.8 @ 41 kW

2.4. Integration of a bipolar LVDC-grid

The connection of an LVDC grid can be made with a direct power conversion from either the MVAC grid or the LVAC grid in a single power conversion stage. Alternatively, the grid can be connected to a DC-link of the ST. In the latter case, the ST can control the power flow between all grids and enables to isolate disturbances in the grid in which they are occurring. For the LVDC grid, the ability to provide bidirectional power flow is essential, because energy storage systems, distributed generation systems (like PV converters) and electric vehicle charging stations may be connected to it.

For the design of the LVDC grid, the authors of this work have found a lack of applicable norms with respect to voltage level, isolation requirements and protection systems. Therefore, it is required to take into account the requirements of the LVDC operator and the connected loads. This may require galvanic isolation of the DC grid, but is not absolutely mandatory. As an example, EV charging stations are required to provide galvanic isolation to the cars and therefore, the grid may not be isolated. If other DC loads are connected, which are not galvanically isolated, it is likely that the grid needs to be isolated.

As another open point, the grid voltage of the LVDC grid needs to be defined. Generally, there are conflicting goals for the optimization of the system. The maximization of the DC-grid voltage is desired for the purpose of increasing the line capacity, whereas a reduction of the grid voltage brings advantages for safety and potentially efficiency. As an example for a grid with an AC voltage of 400 V, the expected LVDC-link voltage should be in the range of 700…800 V. Thereby, the maximum LV-voltage for the grid is 1.5 kV and brings the maximum grid capacity, but a voltage transfer ratio of 2 is expected to result in lower efficiency than a unity voltage transfer ratio. The

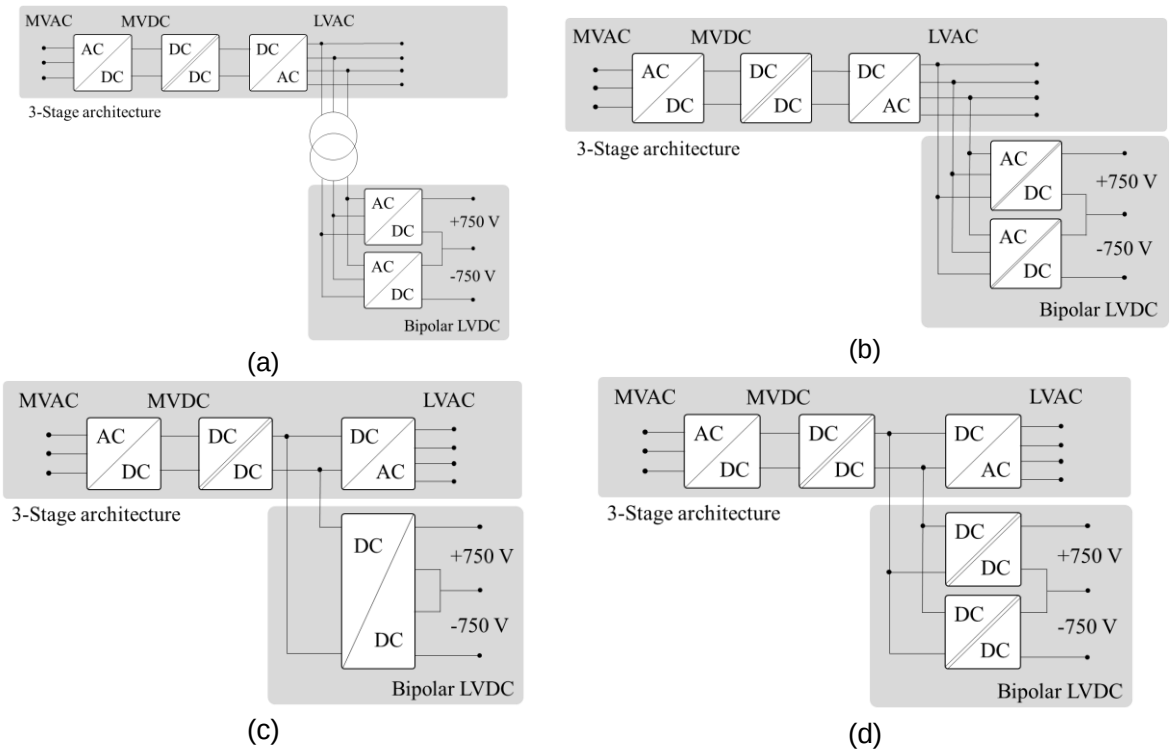


Figure 12: Three-stage architecture with a bipolar LVDC connectivity; by (a) non-isolated AC/DC, (b) isolated AC/DC, (c) non-isolated DC/DC and (d) isolated DC/DC.

LVDC grid can be realized as a unipolar system (positive potential, neutral) and a bipolar system (positive potential, neutral, negative potential). The advantage of the bipolar concept is its natural fault tolerant property and the use of devices with half the blocking voltage with respect to the overall DC-grid voltage. The topologies, which can potentially be used to provide the DC-grid are similar to those ones introduced for the isolation stage of the ST. The bipolar LVDC grid is considered to visualize the different opportunities to realize the LVDC grid as it is shown in **Figure 12**.

The possible architectures can be categorized by the connection to AC or DC and by galvanic isolation of the converter or a non-isolated converter. In **Figure 12 (a)**, the configuration with the non-isolated AC/DC converter is shown, whereas **Figure 12 (b)** shows the isolated converter. In **Figure 12 (c)**, the converter is fed non-isolated from the DC-link and in **Figure 12 (d)**, the converter is isolated from the DC-link.

As discussed before, the galvanic isolation may be required to prevent unwanted current flow due to grid faults between the LVAC and LVDC grid. For this purpose, the isolation may to be required, but it limits the efficiency and the power density if a low frequency transformer is adopted (as shown in **Figure 12 (a)**). The efficiency can be improved by adopting the solution shown in **Figure 12 (b)** However, a critical shortcoming of the AC/DC configurations is that the LVDC grid is highly coupled with the LVAC grid. For example, if a fault occurs in the LVAC side and the LVAC grid is shut down, the LVDC is consequently disabled.

The use of a DC/DC converter connected to the LVDC-link of the converter solves the problem of the coupled grids. This is shown in **Figure 12 (c)** and **(d)**.

2.5. Literature review on possible ST architectures and evaluation of potential services

The application of a power electronics based transformer as the interface between medium voltage and low voltage has been proposed in traction applications, where it was mostly referred to as

"Solid state transformer" or "Power Electronics Based Transformer". Several companies have proposed architectures and designed systems, which are introduced and discussed in the

following. A matrix converter based architecture is shown in **Figure 13**. It is based on a single

power conversion stage, which does not provide DC-connectivity and therefore, it may be limited in decoupling the grids. However, it is capable to provide grid services such as the reverse power flow and the reactive power support. A challenge of matrix converters in general is a complex combination of the switching states. If Sinusoidal Pulse Width Modulation (SPWM) is used, there is a limitation in the maximum modulation index, which can be used (up to 87%). This is limiting the utilization of the hardware. Another challenge is the protection in case of an immediate turn off because of the lack of a freewheeling path for the current. In comparison with other topologies, the transformer is fed by hard switching power semiconductors on the low voltage side, which limits to achieve a higher efficiency. Another challenge, which the authors of the proposed topology identify are the limitation of common mode voltages [10].

Another possibility to realize matrix converters is to use two stages with an additional DC-link as shown in **Figure 14**. **Figure 14 (a)** shows the system proposed by ABB with series connected building blocks on the MV-side and parallel connected H-bridges on the low voltage side. The medium voltage side is referred to as a cycloconverter and synthesizes its output waveform without a DC-link. The system operates similar to a matrix converter, but provides DC-connectivity and thereby the AC grids can be decoupled. As a challenge of this topology, the trade-off between limited power semiconductor losses and high frequency for the transformer needs to be determined. In **Figure 14 (b)** an architecture is realized with a single building block (without modularity).

A single power conversion stage based ST architecture, which is expected to achieve high efficiency is the unfolding bridge based topology shown in Error! Reference source not found.. The u nfolding bridges operate with the fundamental frequency and a medium frequency transformer, a series resonant converter in this case, is providing galvanic isolation and transfers the power. In this architecture, the unfolding bridge is on both AC-sides, whereas it is also possible to apply it only on one of the two AC-sides.

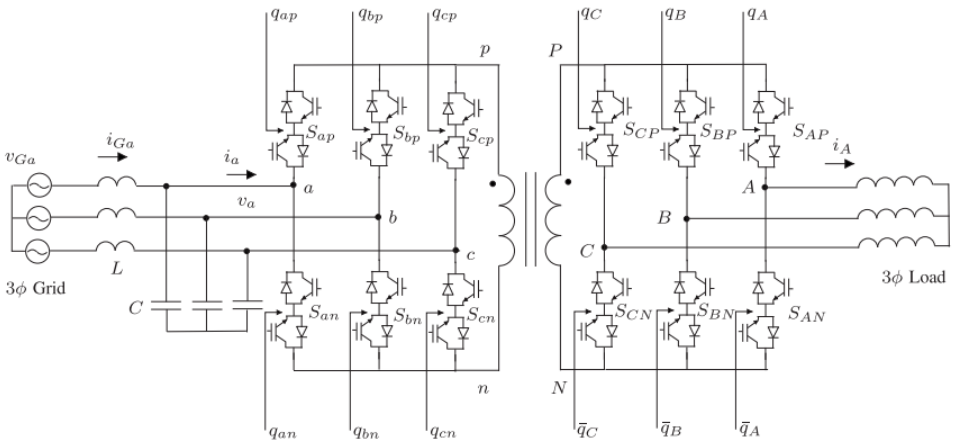
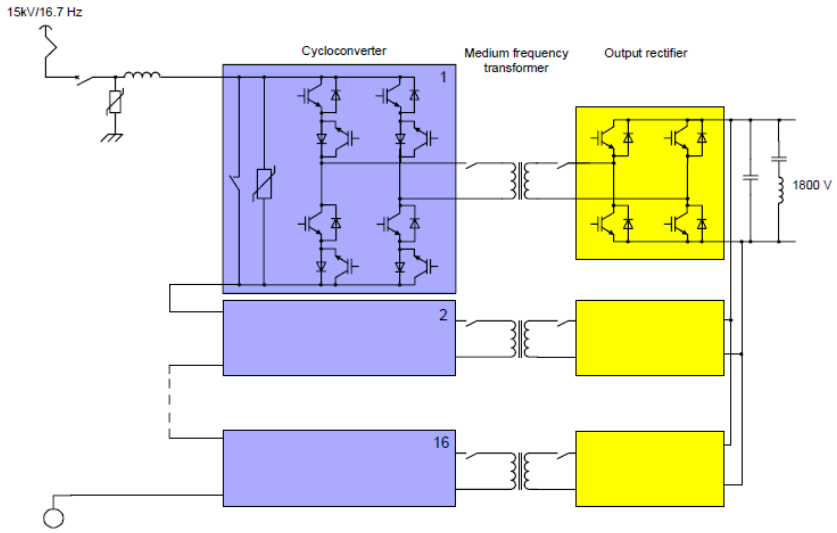
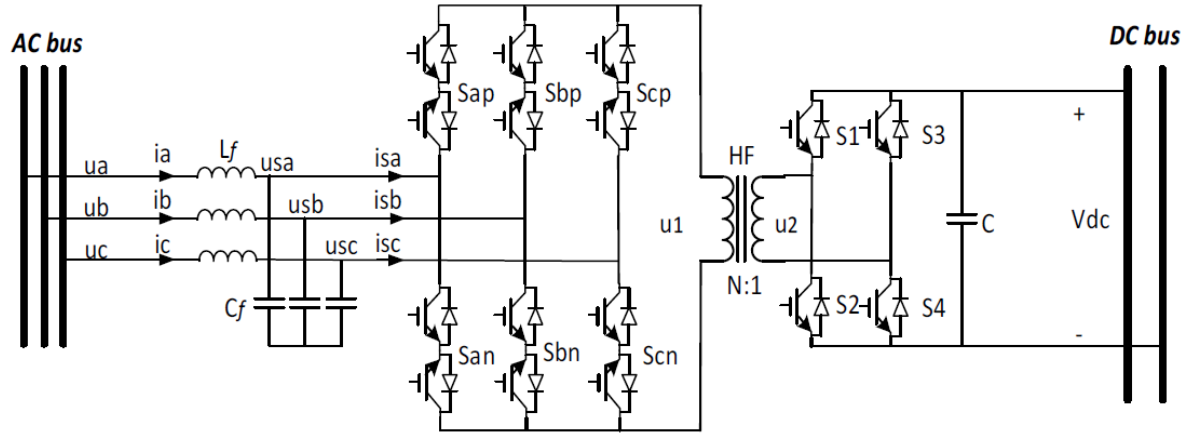


Figure 13: 1-stage configuration by University of Minnesota: (MVAC) Matrix -(TR)-Matrix (LVAC) [10].



(a)



(b)

Figure 14: 2-stage configuration by (a) ABB [11], (b) University of Alberta [12]: (MVAC) Matrix-(TR)-Rectifier (LVDC).

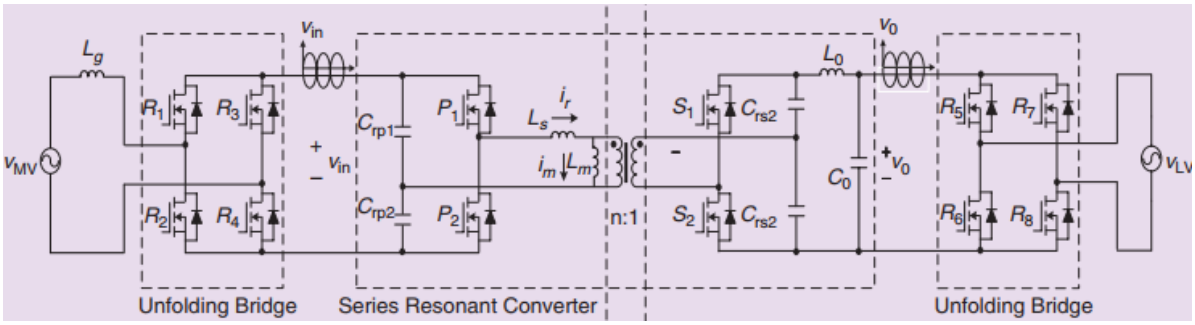


Figure 15: 1-stage configuration by FREEDM [13]: (MVAC) Unfolding -SRC (TR)- Unfolding (LVAC).

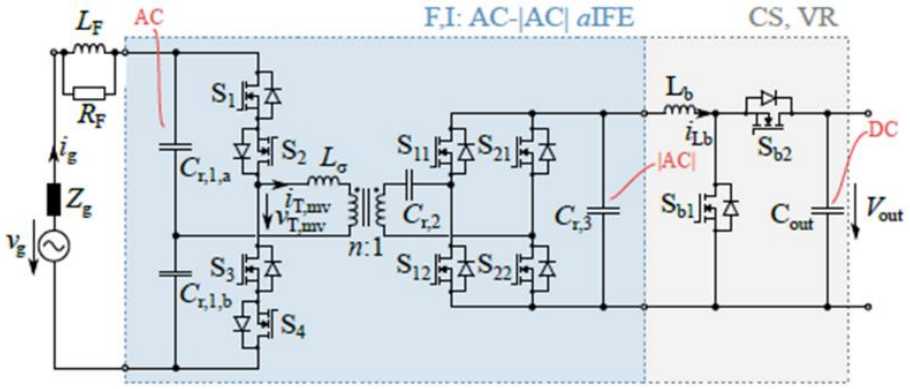


Figure 16: 2-stage configuration by ETH [14]: (MVAC) Unfolding -(TR)-DC/DC (LVDC).

In **Figure 16**, the unfolding bridge is only applied in the medium voltage side and DC-connectivity is provided in the low voltage side. This architecture has the advantage of simplicity on the medium voltage side, whereas the low voltage side is complex to be controlled. Remarkably, in the medium voltage side, the resonant tank (L_F and C_r) is used to achieve soft switching for the whole operation range. However, since the pulsating current has a higher amplitude, power devices with a higher rated current are required and the efficiency is worse in the high power operating range due to higher conduction losses.

Modular three-stage converter architectures are shown in **Figure 17**. The advantage of those architectures is the modularity on the cell level and potentially inherent redundancy. In addition, it is possible to independently choose the topology for the stages and to have the full controllability for grid services. As another advantage, two DC-links are separating the AC-grids, which is expected to provide improved decoupling of the two grids. The disadvantage of these topologies is a high switch count and the need for DC-links with a high capacitance.

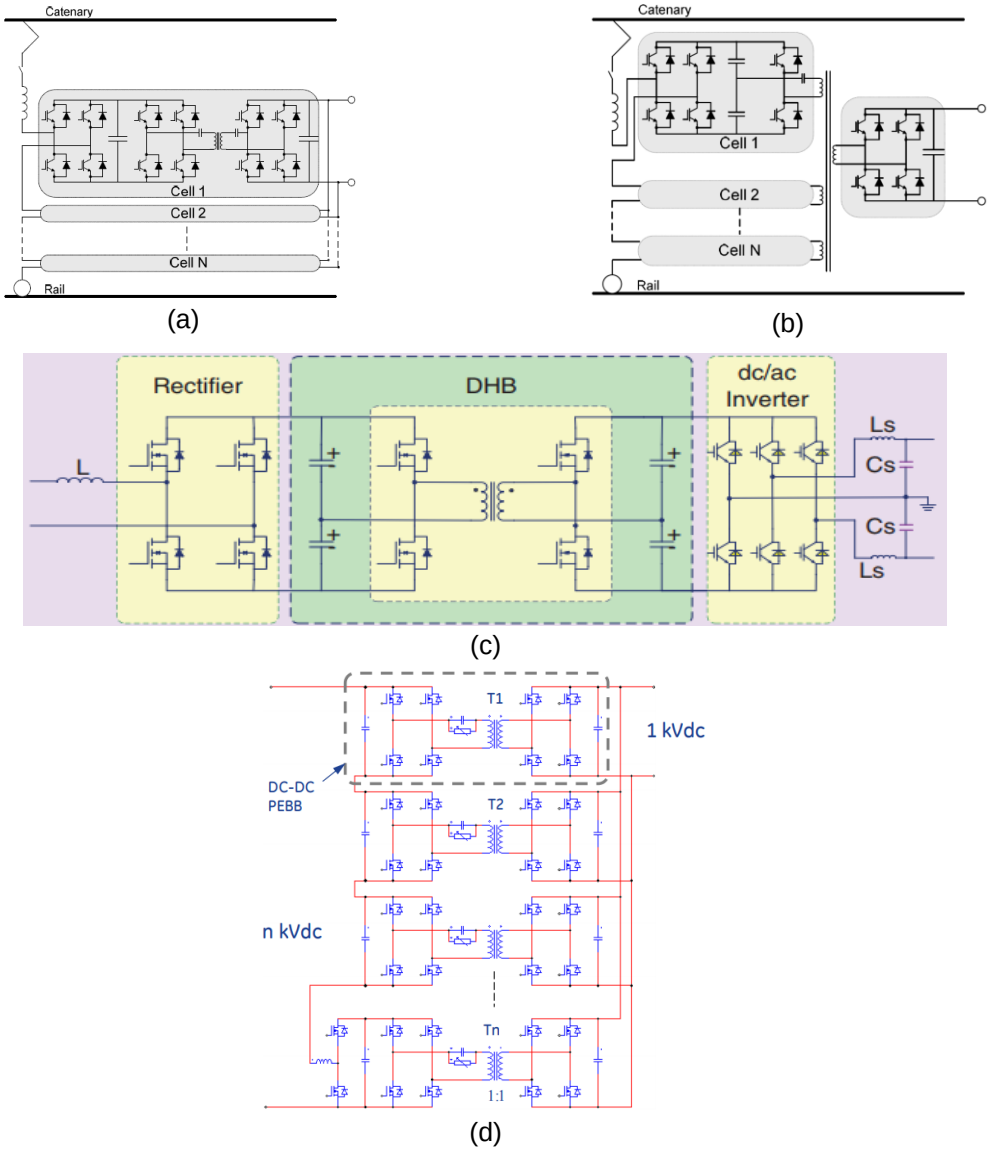


Figure 17: 3-stage configuration: (a) (MVAC) CHB -SRC (LVDC)-(LVAC) [15],[16] ,[17](b) (MVAC) CHB-Semi-modular SRC (LVDC)-(LVAC) [18] (c) (MVAC) CHB-DAB (LVDC)-(LVAC) [13] (d) (MVAC) Modular-(MVDC) Cascaded SRC (LVDC)-(LVAC) [19].

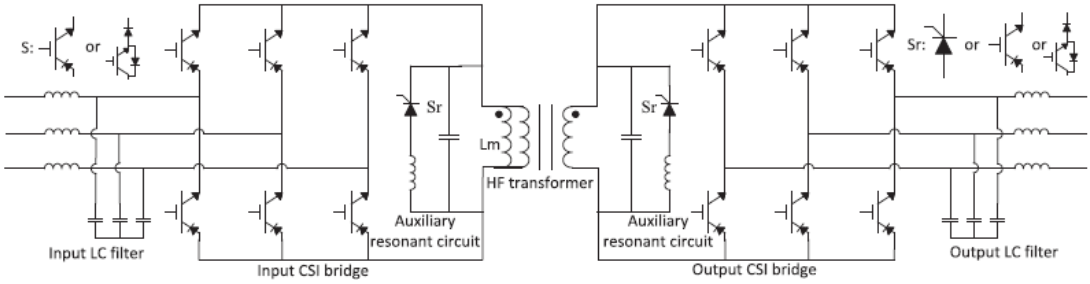


Figure 18: (MVAC) Current source-resonance circuit-current source (LVDC) [20].

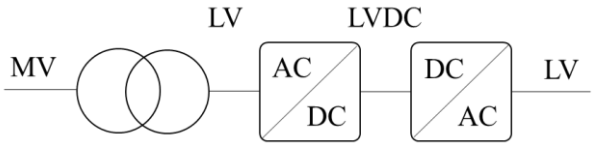


Figure 19: Concept of a back-to-back converter based ST.

Another opportunity to realize an ST is to use current fed topologies as shown in **Figure 18**. This does not provide DC-connectivity, but it does not require DC-link capacitors. Instead, the energy is stored magnetically (inductors). As shown in the figure, auxiliary circuits are required for soft switching. It does not affect inrush currents, but the transformer size is expect to be 50% bigger than in a DAB for the same power. The topology enables to provide grid services and bidirectional power flow.

Table 2: Comparison between three stages ST and back-to-back converter with transformer: + superior/good performance, 0 neutral, - worse/inferior performance.

	Back-to-back with transformer	Three stages ST
Size and weight	-	+
Functionality	+	+
Efficiency	0	0
Development costs	+	-
Material costs	+	-
Disturbance rejection	0	+
DC-link access	0 Only LV possible	+ LV and MV possible

An alternative to the ST architectures without the high-frequency isolation is the use of a standard transformer and a back-to-back converter in the low voltage side as shown in **Figure 19 (a)**. This architecture provides DC-connectivity, bidirectional power flow and grid services for both AC-grids. In comparison with a three-stage ST architecture, it is expected to be considerably less expensive, because of the existing experience for PV/wind turbine applications. A comparison between the two solutions is shown in **Table 2** by means of size & weight, functionality, efficiency, development costs, material costs and disturbance rejection capability. The functionality of both solutions is similar and both architectures can perform independent voltage control in case sufficient active power is provided. For the comparison of the efficiency, a simple test case was made in a conference paper, where the ST was concluded to obtain superior efficiency in partial load operation (below 50%) [21]. However, this is comparison is highly dependent on the considered components and may change accordingly. Apart from this, the material costs and the development costs for the ST are expected to be higher. The disturbance rejection capability is referring to the decoupling capability of the two AC grids, referring to the influence of a disturbance on the other ac grid. As an example, an overvoltage or a voltage sag in one of the grids should not affect the other grid and potentially violate the voltage regulations. Therefore, it is advantageous to have more than one DC-link to limit the influence of one grid on the other grid. Consequently, the three stage solution is expected to be superior, because of the two DC-links, which are achieving a better decoupling of the grids compared to the single DC-link. The availability of the DC-links is also limited for the B2B converter with its single DC-link, whereas the SST can enable to provide MVDC-link.

Table 3: ST architectures and their influence on the modularity, DC-connectivity and applicability to the LV Engine schemes.

Architecture	Number of power conversion stages			Modularity (system, topology or cell level)	Applicability for LV Engine schemes					DC connectivity		References
	1	2	3		1	2	3	4	5	MV	LV	
Indirect matrix converter	1 (MVAC-LVAC)			Cell, system level	x	x	x	-	-	-	-	[22]
LF unfolding bridge+current source SRC+LF unfolding bridge	1 (MVAC-LVAC)			System level	x	x	x	-	-	-	-	[13]
Cascaded cycloconverter + 2 level VSC		2 (MVAC-LVDC-LVAC)		Cell, system level	x	x	x	x	x	-	x	[11]
Isolated AC-DC matrix converter		2 (MVAC-LVDC-LVAC)		System level	x	x	x	x	x	-	x	[12]
Soft switching current source converter		2 (MVAC-LVDC-LVAC)		Cell, system level	x	x	x	x	x	-	x	[20]
Unfolding bridge+DC/DC converter		2 (MVAC-LVDC-LVAC)		Cell, system level	x	x	x	x	x	-	x	[14]

Back-to-back converter plus transformer	2 (LVAC-LVAC + transformer)	Topology, system level	x	x	x	x	x	-	x	-
CHB+SRC+2 level VSC	3 (MVAC-MVDC-LVDC-LVAC)	Cell, system level	x	x	x	x	x	-	x	[15],[18] ,[16]
CHB + DAB+ 2 level VSC	3 (MVAC-MVDC-LVDC-LVAC)	Cell level, system level	x	x	x	x	x	-	x	[23]
CHB+SRC+3 level NPC	3 (MVAC-MVDC-LVDC-LVAC)	Cell, system level	x	x	x	x	x	-	x	[17]
Cascaded SRC	3 (MVAC-MVDC-LVDC-LVAC)	topology level, system level	x	x	x	x	x	x	x	[19]

Theoretically, a medium frequency transformer can be added to the back-to-back converter and thereby provide the second DC-link access. This results in lower expected costs compared to the three-stage realization, but is not desired, because it will produce disadvantages with respect to volume and efficiency compared to the other solutions.

The selected architectures are grouped in dependence of the previously introduced categories of modularity and the number of power conversion stages. Regarding the modularity, it is highlighted on which level the topology/architecture enables to apply modularity:

- Building block level (cell level)
- Topology level or
- System level.

Thereby, the cell level enables to scale up/down the rating of the voltage or power with cells (e.g. link H-bridges) and is the highest level of modularity, which can be achieved. The topology level refers to the modularity on the topology level, which enables to increase the power level by adding (similar) topologies in parallel. The system level is the lowest level of modularity and only enables to parallel similar architectures for increasing the power rating.

The applicability of the architectures to the five LV Engine schemes is marked and the availability of DC-links. The comparison between the topologies is shown in **Table 3**. As a general conclusion, the direct matrix converters do not provide DC-link access. Therefore, they are not suitable for the LV Engine schemes 4 and 5. However, for the application of the LV Engine schemes 1, 2 and 3 they are applicable.

The two-stage architectures obtain LVDC-link access and they are applicable to all LV Engine schemes. For the three-stage architectures, several of them do not have MVDC-connectivity, because of the use of distributed DC-link. Nevertheless, the distributed DC-link of the CHB-converter on the MV-side helps anyway to the decouple the grids. If the MMC is applied in the MV-stage, the MV DC-connectivity is provided.

Table 4: ST architecture and their impact on potential grid services: * Cannot control the reactive power in MV-side and LV-side independently, ** can be achieved with for a limited range at the expense for a significantly higher THD.

Architecture	Number of power conversion stages	Services					
		MV DC	LV DC	Q-control in MV	Q-control in LV	Power flow control	Harmonic filtering
Indirect matrix converter	1	-	-	(x)*	(x)*	x	-
LF unfolding bridge+current source SRC+LF unfolding bridge	1	-	-	(x)**	(x)**	-	-
Cascaded cycloconverter + 2 level VSC	2	-	x	x	x	x	x
Isolated AC-DC matrix converter	2	-	x	x	x	x	x
Soft switching current source converter	2	-	x	x	x	x	x
Unfolding bridge+DC/DC converter	2	-	x	x	x	x	x
Back-to-back converter plus transformer	2	-	x	x	x	x	x
CHB+SRC+2 level VSC	3	-	x	x	x	X	x
CHB + DAB+ 2 level VSC	3	-	x	x	x	X	x
CHB+SRC+3 level NPC	3	-	x	x	x	X	x
Cascaded SRC	3	x	x	x	x	X	x

The capability for grid service such as the reactive power support in the MV and LV grids and the power flow control is evaluated in **Table 4**. Grid services are considered as the capability for bi-directional power flow and reactive power control in both connected AC grids.

All of the three-stage and two-stage configurations can provide the considered grid services, whereas the single-stage configurations only provide the bidirectional power capability. The indirect matrix converter can provide reactive power control, but this may also influence the AC grid on the other side, which is not desired. However, the capability of the grid services may depend on the control strategy and recently, in [24], a reactive power control for the single-phase grid-tie unfolding inverter in PV application was proposed. This method modifies a shape of the grid current waveform in order to control the power factor, keeping the zero crossing point synchronized with the grid voltage. However, the THD of the current is increased, because of the modified current shape. By the proposed method, the power factor can be controlled up to 0.86, while the THD is increased by around 30 %. In other words, the configuration in [13] has possibility to provide the reactive power support functionality. However, it has a negative impact on the system performance and the application requires a significant overdesign. Therefore, such advanced control and modulation strategies are not further considered in the comparison.

For the architectures, which adopt a low frequency converter (e.g. back-to-back plus transformer), it needs to be mentioned that the independent voltage control is feasible, but there may be a limitation by the adopted transformer and the resulting impedance, potentially limiting the reactive power injection to the grid.

2.6. Impact of ST architecture on estimated costs

The costs for the ST can be split into different sub-costs, which are generally hard to quantify for different manufacturers, especially if some of the systems can be adopted from existing products, whereas other systems need to be developed from scratch. Therefore, the hardware costs in dependence of the topology are estimated qualitatively in this work. As major part of the costs, the power semiconductors stand out in the costs of a converter. However, it is a challenge for the modular systems to define the optimal number of building blocks in consideration trade-off between a high number of power semiconductors and the high costs for power semiconductors with high blocking voltage. Thereby, also the power semiconductor technology has an impact on the costs. Moreover, the design influences the cost of output filters, particularly on the medium voltage side, communication within the system and software development costs. The latter one is affected for the controller design, modulation of the converter and potentially a controller with the required communication capability.

As a design parameter in modular power converter topologies, the number of building blocks *n* can be used to reduce the switching frequency of the single power semiconductor as shown in (1):

$$f_s \sim \frac{1}{n^2} \tag{1}$$

A higher number of building blocks enables to reduce the switching frequency of the single power semiconductor in the building block as it is expressed with this equation. This equation assumes similar output current ripple. Therefore, the reduction of the switching frequency can be used for two different goals:

1. Actual reduction of the switching frequency to reduce the losses and therefore reduce the cooling system requirements
2. Reduction of the filter requirements by increasing the effective switching frequency of the converter

The second point, the reduction of the output filter, is realized by increasing the actual switching frequency of the converter. Consequently, the filter size can be reduced as expressed with (2):

$$L_{min} \sim \frac{1}{f_s} \tag{2}$$

Taking into account the introduced converter architectures and the design trade-offs potentially available through the modularity, an overview and a comparison is shown in **Table 5**.

Table 5: ST architecture and their impact on the system design with n as the number of modular building blocks.

Architecture	Number of semiconductors per building blocks (MV-stage, isolation stage, LV-stage)	Device rating (MV stage, isolation stage, LV-stage	AC filter requirements for MV-side	Software design effort	Overall estimated Costs
Indirect matrix converter	6	HV	1	High	Low
	-	-			
	4	LV			
LF unfolding bridge+current source SRC+LF unfolding bridge	4*3	HV	1	Low	Low
	4*3	HV			
	4*3	LV			
Cascaded cycloconverter + 2 level VSC	12*n*3	LV	1/n	High	Medium
	8	LV			
Isolated AC-DC matrix converter	12	HV	1	High	Low
	Flexible (8)	LV			
Soft switching current source converter	12	MV	1	Medium	Medium
	12	LV			
Unfolding bridge+DC/DC converter	8*3	LV	1	High	Medium
	2	LV			
	Flexible (8)	LV			
CHB+SRC+2 level VSC	4*3*n	LV	1/n	Medium	Medium
	8*3*n	LV			
	8	LV			
CHB + DAB+ 2 level VSC	4*3*n	LV	1/n	Medium	Medium
	8*3*n	LV			
	8	LV			
CHB+SRC+3 level NPC	4*3*n	LV	1/n	Medium	Medium
	8*3*n	LV			
	18	LV			
Cascaded SRC (DC/DC)	Flexible	LV	Flexible	Medium	High
	8*3*n	MV/LV			
	flexible	LV			
2 LV converters + transformer	8	LV	-	Low	Low
	8	LV			

The number of power semiconductors is evaluated based on a three phase architecture and it is highlighted, if high voltage or low voltage devices are required. Thereby, high voltage devices have the advantage of requiring a lower number of devices, but they are generally much more expensive. The filter requirements are shown only for the MV-side, whereas it is highlighted if a modular design enables to reduce the size of the filter. Thereby, it needs to be mentioned, that this filter may needs to be sized for several hundreds of mH (for a L-filter), if a lower number of voltage levels are produced. The software design is considering the complexity of the control for the architecture and the mandatory communication requirements. Finally, the overall evaluation is made based on all facts analyzed before.

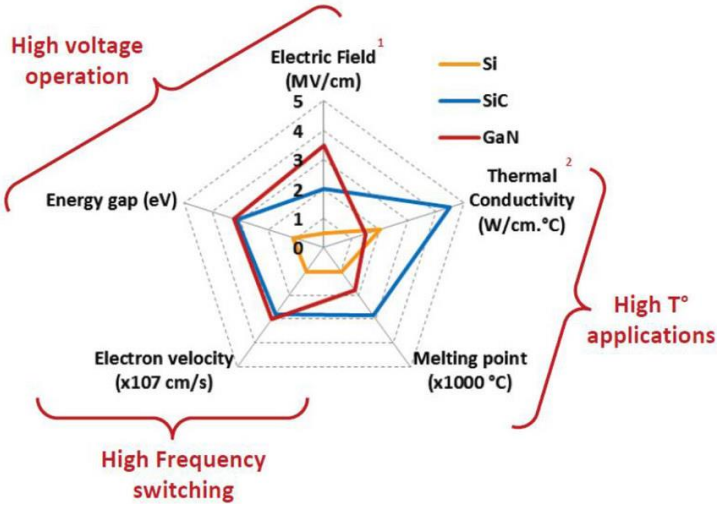


Figure 20: Comparison of different power semiconductor technologies [25].

2.7. Selection of suitable components for the converter stages

This section reviews commercial products by means of their costs and efficiency, discusses potential power semiconductor technologies and potential core materials for the medium frequency transformer and its impact on the costs and performance of the system.

2.7.1. Impact of power semiconductor technology

The power semiconductors consisting of Silicon (Si) are well consolidated in the market and the improvement of their performance is continuously ongoing. However, there are technological barriers with respect to the efficiency, which Si-based power semiconductors will not overcome. Therefore, other power semiconductor materials are being investigated to reduce further the losses of the power converters. The most prominent examples are Silicon Carbide (SiC) and Galium Nitride (GaN). For comparison of the technology, **Figure 20** compares several physically important benchmark parameters, which are the electric field strength, the energy gap, the electron velocity, the melting point and the thermal conductivity. As it can be seen, the wide-bandgap devices outperform the Si-based power semiconductors. Remarkably, SiC is expected to be promising for high voltage operation, whereas GaN is currently only available for relatively low voltage rating. Therefore, apart from the consolidated Si-based power semiconductors, SiC is currently the more promising power semiconductor material.

As it can be seen in **Figure 20**, the melting point for the wide-bandgap devices is much higher than for the Si-devices. However, the maximum operating temperature is not limited by the melting temperature of the power semiconductor material, but on the packaging technology. This is commonly limited by the solder material and the maximum operation temperature of Si-devices and SiC devices is product dependent. Commonly, the maximum operating temperature for Si-devices and SiC devices is 150°C, 175°C or 200°C. However, these are overall maximum ratings, which should not be used for continuous operation. The designed maximum temperature is having an impact on the lifetime of the power semiconductors and therefore, usually the mission profile and the operation time of the lifecycle is analysed. As a rule of thumb, an increase of the operation temperature by 10°C results in halving the lifetime of the power semiconductors.

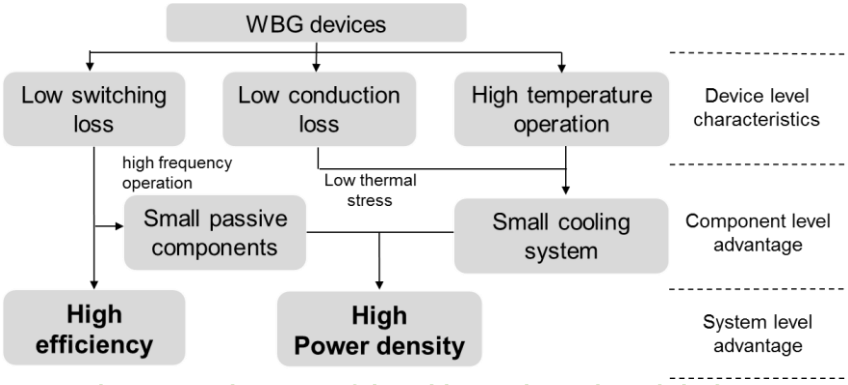


Figure 21: Advantage of the Wide Band-Gap (WBG) devices.
(source: FREEDM "Wide Band-Gap Devices for Solid State Transformer Application")

Wide Band-Gap (WBG) devices: advantages, disadvantages:

Characteristics of the WBG devices are shown in **Figure 21**. Compared with Si-IGBT, the WGB devices feature lower switching losses, which enables the converters to operate with a higher switching frequency. Consequently, this enables a lower rating of passive components and it can contribute to achieve high power density. The latter point is also enabled by reduced losses, which requires less effort for the cooling system. A potential for the future is the operation with higher temperature, which can also significantly contribute to achieve high power density.

Prospect of WBG devices development:

As it can be seen in **Figure 22 (a),** the Si based devices technology is mature for up to 6.5 kV blocking voltage and 5 kHz of switching frequency, whereas the SiC based devices technology has a potential for the high blocking voltage up to 20 kV or higher at the fast switching frequency above 20 kHz.

From an economical perspective, it is predicted that the price of WBG devices will be competitive with Si based devices within a few years as shown in **Figure 22 (b)**, where the horizontal axis is the year from 2016 to 2020 and the vertical axis is the price per ampere.

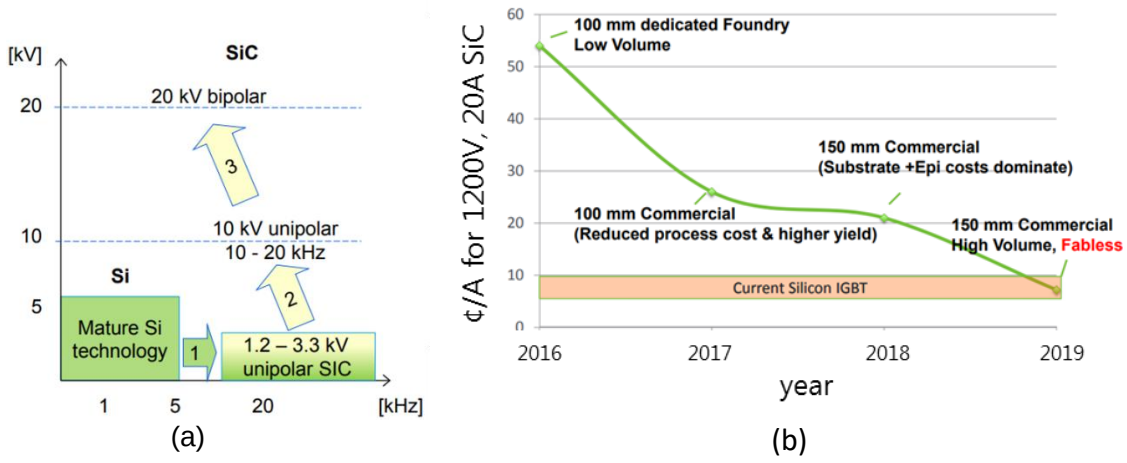


Figure 22: Prospect for (a) development and (b) price of SiC devices.
(source: ABB "MV WBG Power Electronics for Advanced Distribution Grids," NIST/DOE Workshop, 2016 and US department of energy "Wide Bandgap Device Manufacturing," NIST/DOE workshop, 2016).

Comparison between Si-devices and a SiC MOSFET:

Table 6: Comparison of the general performance between Si-based devices and SiC based devices.

Power semiconductor technology	Efficiency impact	Switching frequency	Device robustness	Technology maturity	Costs
Si-IGBT	-	-	+	+	+
Si-MOSFET	0	0	+	+	+
SiC-MOSFET	+	+	-	0	-

In **Table 6**, the characteristics of a SiC-MOSFET are compared with the Si-IGBT and Si-MOSFET by means of efficiency, maximum switching frequency, device robustness, technology maturity and device costs. The SiC-MOSFET shows a better performance in terms of the efficiency, temperature, power and switching frequency, but the others have the advantages in terms of reliability and costs.

Before discussing suitable power semiconductors for each stage, the challenges of the different converter stages are discussed in the following:

Challenges for the MV stage:

The major challenge is the blocking voltage capability for the medium voltage and the commercially available devices. For Si-IGBTs, the highest blocking voltage in the market is currently 6.5 kV. Here, it needs to be considered that this is not the operating voltage, because a certain de-rating to ~50-75% of the blocking voltage required preventing cosmic ray induced failures. For example, 1.2 kV devices are adopted for 600 ~ 800 V applications.

Another challenge of the Si-devices with high blocking voltage is the low maximum switching frequency and high switching energy. The limited switching frequency is a bottleneck in reducing the passive filter size/weight and the bigger filter size causes a higher voltage drop, leading to a higher minimum DC-link voltage.

Challenges for the isolation stage:

This stage plays a role as a link between the MV and LV stages, providing a galvanic isolation through a high/medium frequency transformer. The major bottleneck is the design of the transformer by ensuring a high efficiency and power density. Hence, a high switching frequency is expected, which results in higher switching losses.

As a particular challenge, the MV side operates for a high voltage and low current, which leads to a required high blocking voltage capability, whereas the LV side operates for a lower voltage and higher current.

Challenges of the LV stage:

This stage features conditions, which are well known from gird connected converters for the integration of renewable energy, such as PV converters. This knowledge and experience can be adopted.

Recommendation of proper device technology for each stage:

Table 7: ST stages and the impact of the power semiconductor technology.

Stage	Power semiconductor technology	Advantages	Disadvantages	Recommendation
MV-stage	Si-IGBT	Low conduction loss	Limited blocking voltage	Si-IGBT, potentially differentiate with respect to modularity
	Si-MOSFET		Not suitable	
	SiC-MOSFET	High blocking voltage Low switching loss	Reliability and cost	
Isolation stage	Si-IGBT	Reliability and cost	Limited efficiency, low switching frequency	MV-side: SiC-MOSFET LV-side: Si-IGBT
	Si-MOSFET	Reliability and cost	Limited power capability	
	SiC-MOSFET	High switching frequency	Reliability and cost	
LV-stage	Si-IGBT	High current capability and low conduction loss	Limited switching frequency	Si-IGBT
	Si-MOSFET		Limited power capability	
	SiC-MOSFET	Low switching loss	Reliability and cost	

Under consideration of the specific challenges of the power semiconductor technology and the challenges in the different converter stages, recommendations for the use of the power semiconductors are provided in **Table 7**. The Si-MOSFETs are only suitable to be used in the isolation stage, but unfortunately, they are only available with a relatively low current rating. The Si-IGBT has its advantages in low conduction losses, especially at high current ratings. Therefore, Si-IGBTs are recommended to be used in the MV stage and the LV stage – if no isolation is adopted in the same stage. The SiC MOSFET instead is recommended to be used in the isolation stage, where a high switching frequency is desired. In the LV-side of the isolation stage, IGBTs can be applied and result in lower costs, but reduced expected efficiency.

The recommendations are only given for a three-stage configuration in this document. However, the challenges in terms of high blocking voltage/required high switching frequency remain the same – even for the single stage ST architecture.

2.7.2. Expected efficiency for the three different stages

This subsection reviews commercially available power converters, which can be applicable for the ST. For the LV-side converter, PV converters are reviewed, for the MV-side MV converters, mostly for drives, are reviewed and for the isolation stage a study is carried out about potentially suitable designs and their costs.

LV-side (benchmark: photovoltaic-converter)

The efficiency of the LV-side converter is evaluated by a comparison of commercially available photovoltaic converters. From 5 major manufacturers of the solar inverters (rated power from 255 to 2200 kVA), the specifications such as DC-link voltage, output AC voltage, rated power and efficiency are listed in **Table 8**.

For a comparison of the efficiency vs the power rating, **Figure 23** is introduced. As it can be seen, the efficiency ranges from 98 to 98.6 % and there is no strong correlation between the efficiency and the rated power. Consequently, for the ST application, it would be reasonable to target a peak efficiency 98.5 % for the LV-side converter.

Table 8: Comparison of the efficiency for commercially available PV converters (reference for the LV-side of the ST ([1] a transformer is used to boost the voltage).

Manufacture	Part number	Max. DC-Link voltage	Max. AC voltage (50/60 Hz)	Rated Power	Efficiency
ABB	PVS800-MWS-1000KW-C	1100 V	36 kV [1]	1000 kVA	Max: 98.6 European: 98.2
	PVS800-MWS-1750KW-C	1100 V	36 kV [1]	1750 kVA	Max: 98.7 European: 98.5
	PVS800-MWS-2000KW-C	1100 V	36 kV [1]	2000 kVA	Max: 98.8 European: 98.6
AEG	Protect PV.250	1000 V	255 V	255 kVA	Max: 98.7 European: 98.5 CEC: 98.5
	Protect PV.500-ID-UL	1000 V	283 V	510 kVA	Max: 98.3 European: 98.1 CEC: 98.0
	Protect PV.630-ID-UL	1000 V	345 V	630 kVA	Max: 98.7 European: 98.0 CEC: 98.0
KACO	XP500-HV TL ID	1000 V	370 V	500 kVA	Max: 98.7 European: 98.5
	Blueplanet 750 TL3 OD	1000 V	370 V	750 kVA	Max: 98.5 European: 98.2
	Blueplanet 1000 TL3 OD	1000 V	370 V	1000 kVA	Max: 98.5 European: 98.3
	2200 TL3 ID	1000 V	370 V	2200 kVA	Max: 98.3 European: 98.0
SMA	Sunny Central 500CP XT	1000 V	310 V	500 kVA	Max: 98.6 European: 98.4 CEC: 98.5
	Sunny Central 630CP XT	1000 V	362 V	630 kVA	Max: 98.7 European: 98.5 CEC: 98.5
	Sunny Central 760CP XT	1000 V	393 V	760 kVA	Max: 98.6 European: 98.4 CEC: 98.5
	Sunny Central 1000CP XT	1000 V	465 V	1000 kVA	Max: 98.7 European: 98.4 CEC: 98.5

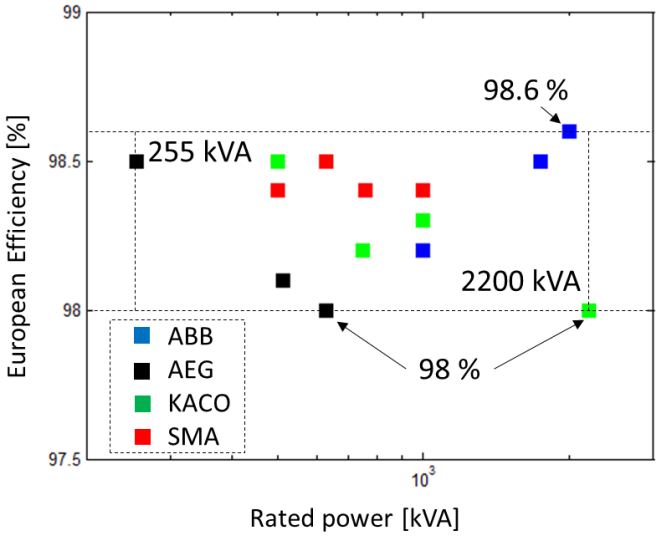


Figure 23: Power vs. European efficiency Curve.

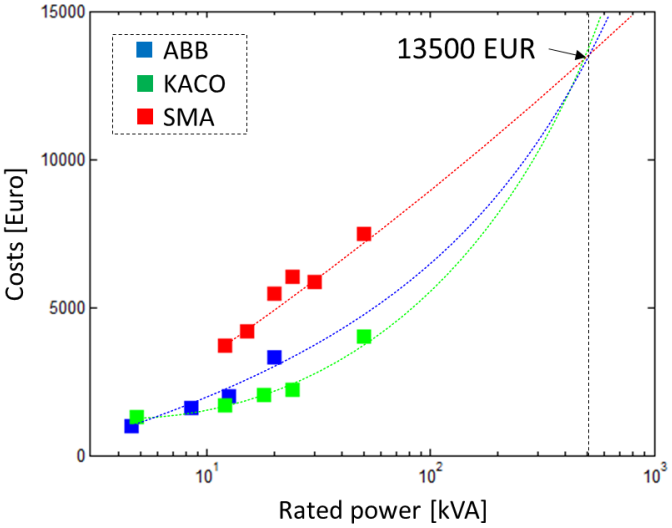


Figure 24: Power vs. Cost.
(https://www.wholesalesolar.com, https://www.photovoltaik4all.de/en)

The cost for the power converter is compared based on information, which is available on websites. Unfortunately, high power systems are not priced in the internet and low power systems are considered and the prices of thee manufacturers are extrapolated for a power rating of 500 kVA. This is shown in **Figure 24** and as it can be seen, the costs are increasing as the rated power is increasing. The dot line is the estimated cost obtained by curve fitting, which concludes that the cost of 500 kVA rated converter is around 13500 EUR. As an alternative source for the price of PV converters, a cost estimation of ~5 cts/Wp for the inverter are estimated [26]. This estimation results in a much higher price of 25.000 € for a converter rated for 500 kVA.

MV side (benchmark MV-converter)

For the MV-side converter in the ST application, commercial products of the medium voltage converters are considered to provide a market overview as shown in **Table 9**. Currently,

applications of commercial MV converter are mostly developed in the field of drives and the AC voltage range is between 2.4 kV to ten kV. Remarkably, the efficiency is between 96.5 to 99 % and has a huge variability.

Unfortunately, there is no pricing information for these systems and therefore, it is not possible to estimate the costs for such a system. However, it is expected to be significantly more expensive than the LV-side converter.

Isolation stage (study case based on component costs)

For the design of the isolation stage, there is a lack of potential products, which can be taken for comparison. Moreover, the design has a huge freedom in the choice of the voltage rating of potentially series connected building blocks. The trade-offs for this designs are shown in **Figure 25**. As the number of cells/modules is increasing, the number of components, such as power devices, is increasing as well and increases the system complexity. This has an additional effect on the control and communication system, which is also getting more complex, but at the same time enables to use power devices with a lower blocking voltage and provide the possibility for fault tolerant strategies. Another point is the filter size and the EMI emissions, which can be reduced with a lower dv/dt in comparison to a lower number of cells/modules.

Table 9: Comparison of the efficiency for commercially available MV-converters (reference for the MV-side of the ST.

Manufacture	Part number	output AC voltage	Rated Power	Topology	Application	Max. Efficiency
Fuji	FRENIC4600FM6e series	6-10 kV	Up to 18300 kVA	Cascased H-Bridge (17 level)	MV drive (fan, pump)	97
GE	MV6 series	2.3-6.6 kV	Up to 3150 kVA	5 level	MV drive	97.5
	MV7000 series	Up to 10 kV	Up to 81000 kVA	-	MV drive	99
HITACHI	HIVECTOL-HVI series	2.4-11 kV	Up to 8800 kVA	Up to 37 level	MV drive	97
Siemens	ROBICON perfect harmony series	4-7.3 kV	Up to 7040 kVA	-	MV drive	96.5
WEG	MVW01 series	13.8 kV	-	-	MV drive	98
Yaskawa	MV1000	4.16 kV	Up to 4500 kVA	Cascased NPC (9 level)	MV drive	97

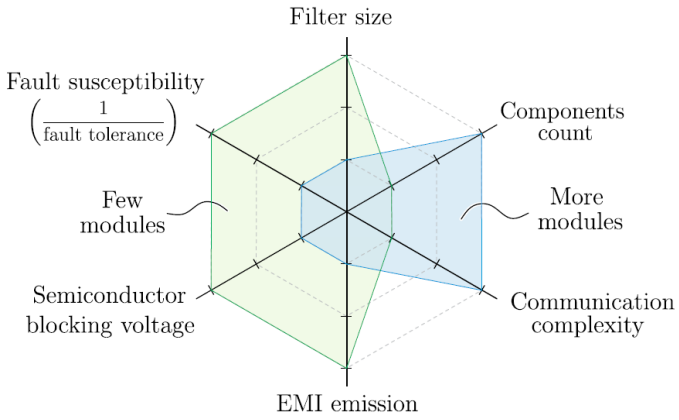


Figure 25: Trade-offs for the selection of the number of cells/modules in a system.

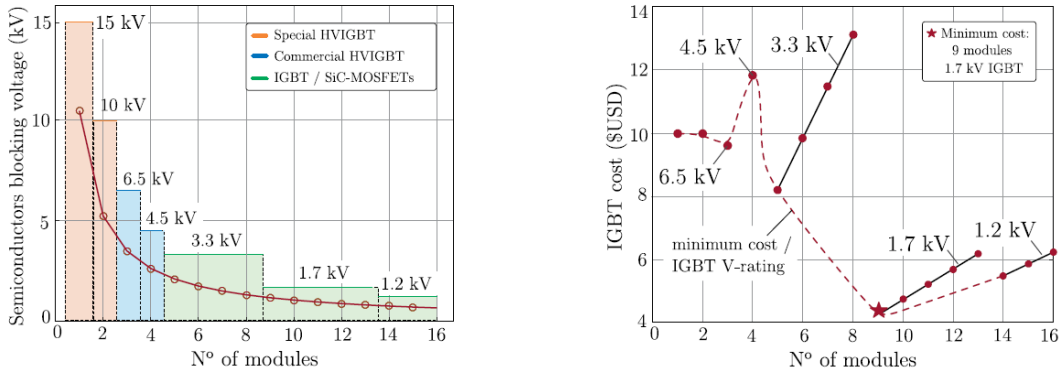


Figure 26: Influence of number of modules on (a) required semiconductor blocking voltage and (b) cost (based on 2017 market price).

The choice of the blocking voltage of the semiconductors is closely related to the number of cells/modules and influence the costs for the devices, whereby the costs for devices with high blocking voltage are usually more expensive than those with a lower blocking voltage. For the design of a QAB, this trade-off is shown in **Figure 26 (a)**, where IGBTs from Powerex and SiC MOSFETs from CREE Wolfspeed are considered. As mentioned before, a lower blocking voltage for the devices requires a higher number of cells/modules. Based on the market prices, the costs for a different number of cells/modules is derived and shown in **Figure 26 (b)**. As it can be seen, 9 cells/modules with a blocking voltage of 1.7 kV is the most cost effective solution.

The trade-offs of the number of modules are used to derive the converter costs, considering costs for power semiconductors, DC-link capacitors, cooling system and auxiliary components (such as gate drivers power supply and control unit). **Figure 27 (a)** shows the system costs as a function of the grid voltage and the number of cells/modules and the optimum number of modules in terms of the system cost is analysed as a function of the grid voltage in **Figure 27 (b)**.

For an evaluation of the correlation of costs and efficiency, the design for the QAB is taken and the costs and efficiency for different power semiconductors is evaluated. Therefore, three combinations of Si and SiC technology are considered for the design of the QAB:

(1) Si for MV and LV,

(2) SiC for MV & Si for LV and

(3) SiC for MV and LV.

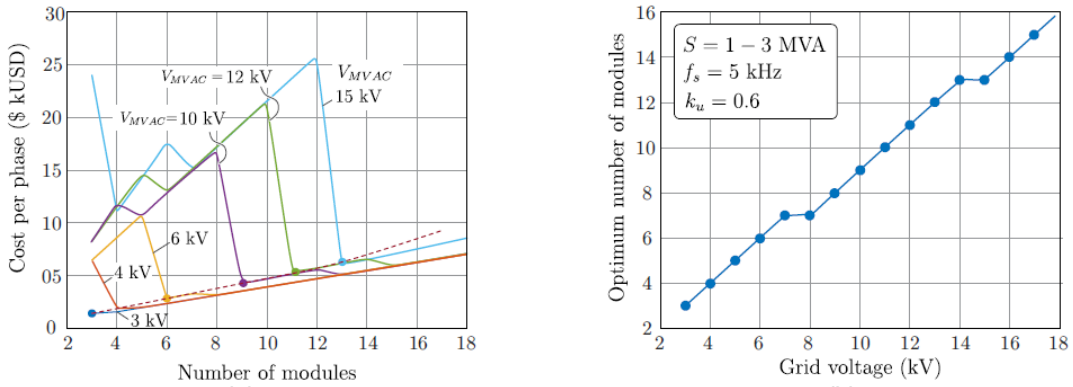


Figure 27: (a) Influence of the number of modules and grid voltage on system cost per phase and (b) optimum number of modules in terms of cost depending on grid voltage.

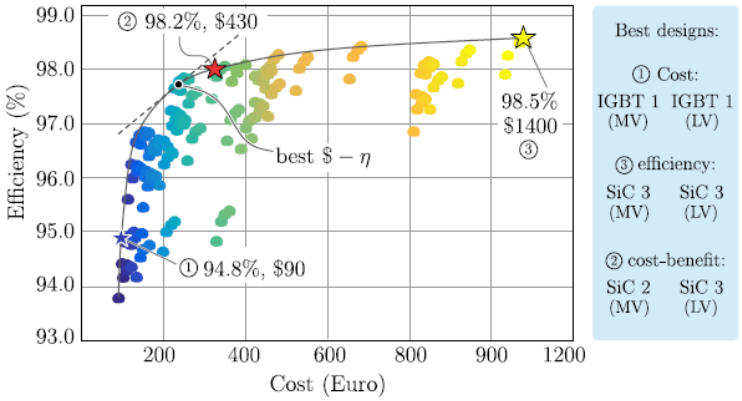


Figure 28: Trade-off between cost and efficiency for the design of a multi-winding DC/DC converter (QAB) [27].

The results of this comparison are shown in **Figure 28**, where a trade-off between cost and efficiency can be observed [27]. As it can be noticed, the lowest cost result in the lowest efficiency and the results are obtained when Si-IGBTs are employed in both side of converter. The SiC based designs provide the best performance, because it has the lowest losses. Depending of the type of SiC devices which are used, the cost can vary in a wide range but the efficiency improvements for the best Sic in class is quite limited. An optimal trade-off can be found as highlighted in the figure around the point 2).

2.7.3. Impact of the cooling solution on the system design

In the ST applications, similar to power converters, the power semiconductor devices, transformers, inductors and capacitors are the major heat sources. The temperatures affect the operating performance and the heat needs to be dissipated. Particularly, the power semiconductors and capacitors are sensitive to high temperatures and their temperature needs to be maintained below the value specified in their datasheet. To achieve this, there are cooling systems for capacitors, inductors and power semiconductors, which are commonly installed. Thereby, the power semiconductors are the most temperature-sensitive devices.

In general, there are two kinds of cooling systems: air-cooling and liquid-cooling, which have been most widely considered, especially for the power semiconductors. An overview about cooling systems is shown in **Figure 29** and the subcategories will be discussed in the following:

Air-cooling system:

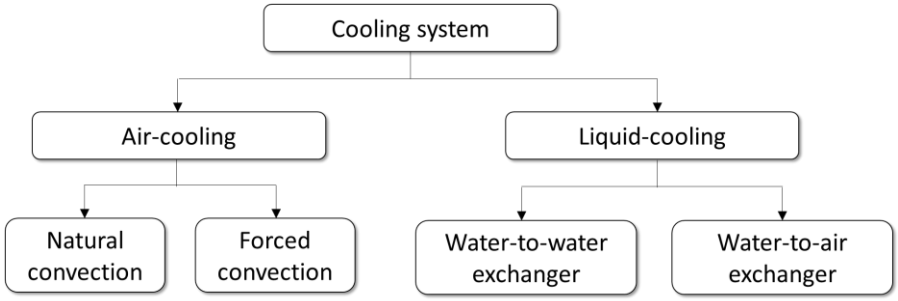


Figure 29: Category of cooling system for power semiconductor devices.

The two kinds of air-cooled systems are shown in **Figure 30**, namely the natural convection cooling and the forced convection cooling. The temperature difference between a heat-sink and the ambient temperature influences the capability for heat dissipation. Hence, the ambient temperature is an important factor to determine the cooling performance and lower ambient temperatures are generally prepared. The air-cooling system can be divided into natural convection and forced convection as shown in **Figure 29**.

In natural convection, as it can be expected from natural, the airflow from the heat-sink to the ambient is achieved by natural convection. Hence, the cooling system is simple and there is no noise from the cooling system with a penalty of low cooling system performance. On the other hand, the forced convection cooling utilizes mechanical fans to blow the air from ambient to the heat-sink fins, where the air is passing through a hot surface of the heat-sink fins and thereby transfers the heat to the ambient. Hence, the forced convection shows a better cooling performance and consequently, it enables a better utilization of the power devices. However, additional mechanical efforts, energy consumption and noises from the fans are the drawbacks.

Apart from the convection, the choice of heat sink is also important in determining the cooling performance, because it is responsible to transfer the heat from the source to the ambient. Generally, cooper and aluminium are considered as the heat-sink materials, whereby the cooper features a higher thermal conductivity, which allows a smaller heat-sink design. However, the cooper is heavier and more expensive. The aluminium instead is lighter and the more cost-effective solution at the expense of a lower thermal conductivity. In addition, arrangement and density of heat-sink fins are other factors to determine the cooling performance, because they determine the contact area and the amount of heat transferred. For the natural convection, a lower number of heat-sink fins with sufficient space between them is used, whereas a higher fin density is considered for the air-forced convection.

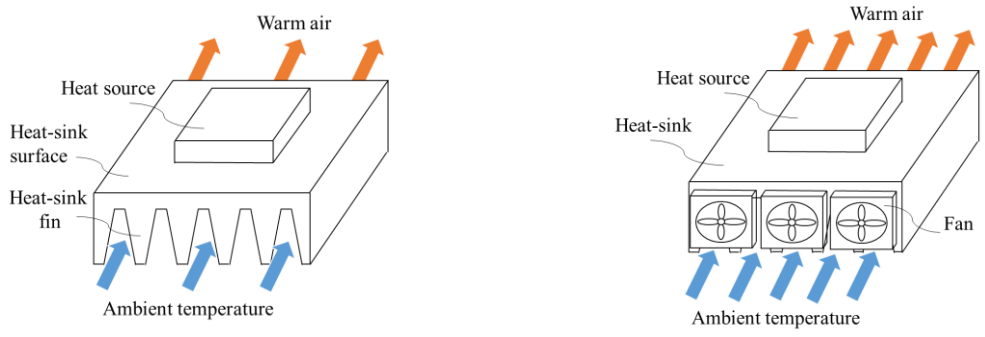
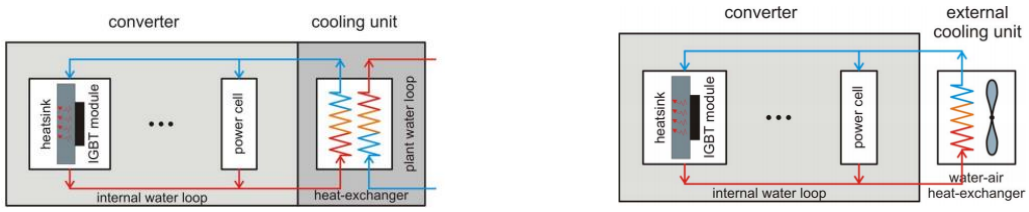


Figure 30: Air-cooling system: (a) natural convection and (b) forced convection system.



(a) (b)

Figure 31: Liquid-cooling system: (a) liquid-to-liquid heat exchanger and (b) liquid-to-air heat exchanger [28].

The ambient conditions such as dust and humidity need to be considered, when adopting the air-cooling system. The heat transfer path due to reduced insulation with dust deposition may cause electrical discharge and failure. It leads to the use of additional equipment, such as dust filter, which increases a regular maintenance (periodic cleaning). It is well-known that humidity is a critical factor for reliability of the power electronics, since an elevated humidity brings reduction of air dielectric capability and the corona effect may be seen in medium voltage application. Namely, the maximum blocking voltage of power semiconductor is also affected by the humidity.

Liquid-cooling system:

The liquid is circulated and transfers the heat from the power semiconductor to the heat exchanger, where the liquid is in contact with the heat-sink. In order to ensure the cooling performance, the liquid has to comply with the temperature requirement and it is commonly kept below 45 °C. Compared with the air-cooling system, the advantage is a higher thermal conductivity (the ability to conduct the heat is roughly 24.5 times higher) and specific heat capacity (the ability to absorb the heat per degree rise is roughly 4 times higher). These characteristics make the liquid-cooling system suitable for high power applications.

The liquid-cooling can be divided in dependence of the heat exchanger: liquid-to-liquid heat exchanger and liquid-to-air heat exchanger [28]. For the liquid-to-liquid configuration shown in **Figure 31 (a)**, there are two liquid loops: one is a closed internal water loop to extract the heat from the power semiconductors and the plant water loop to transfer the heat from the internal water loop to the external water loop without mixing the liquids. The liquid to air configuration uses a single loop for water circulation as shown in **Figure 31 (b)**. The heat is transferred from the power semiconductor devices to water and the heated water is cooled down by ambient air in the heat exchanger with a fan. Hence, the internal water loop is placed with the power converter inside the room, whereas the heat exchanger and the fan are located outside to prevent the ambient temperature increase of the room. Furthermore, it the water needs to be protected from freezing in case the ambient temperature is below zero. This can be achieved by the use of glycol in a mixture with water. However, it could reduce the thermal conductivity and the specific heat capacity of water.

Finally, for some specific applications, where all heat-sinks have different voltage level, the use of deionized water with a low conductivity is desirable, since the liquid circulates in the contact with heat-sink that may be over different voltage potentials. For this purpose, the deionizer filter is required to maintain the low conductivity.

Comparison and performance of the cooling systems

For the comparison of different heat-sink designs, the power density of cooling system can be described by Cooling System Performance Index (CSPI) defined in (3) [29].

$$CSPI[W/(K \cdot l)] = \frac{1}{R_{th,S-a}[K/W] \cdot V_{CS}[l]} \quad (3)$$

Table 10: Typical thermal resistances for air forced cooling and liquid cooling.

Heat-sink			V_{cs} [*l*]	$R_{th,S-a}$ [*K/W*]	CSPI
Air-cooling	Heat-sink size: Fan: Heat-sink material:	80*50*60 [mm³] 2*SanAce Al	0.372 (heat-sink and fan)	0.15	17.9
	Heat-sink size: Fan: Heat-sink material:	40*50*80 [mm³] 1*SanAce Al	0.226 (heat-sink and fan)	0.25	17.7
	Heat-sink size: Fan: Heat-sink material:	40*50*27 [mm³] 1*SanAce Cu	0.120 (heat-sink and fan)	0.27	31.2
Liquid-cooling	-	-	0.037 (only heat-sink)	0.10	270

Where $R_{th,s-a}$ is the thermal resistance from the heat-sink surface to the ambient and V_{cs} is the cooling system volume. It should be noted that the CSPI is independent from power converter efficiency and temperature levels.

In **Table 10**, the CSPI values of four different heat-sink designs is shown. By comparing the first two heat-sinks, it can be seen, that the second one has smaller volume (by a factor of 2) and only one fan is used in contrast to the first heat-slink. This leads to a higher thermal resistance, whereas the volume is reduced. Hence, the CSPI for both shows similar value since the volume and the thermal resistance compensate each other in this case. However, the influence of the heat-sink material can be noticed from the comparison of the second and third design. Thereby, the first and second heat-slink are made by Al, whereas the third is made by Cu. Since the thermal conductivity of Cu is better than that of Al, the volume of the third on can be reduced, whereas the thermal

resistance is similar to the second heat-sink. Consequently, the CSPI of the third one is around 2 times higher, meaning that its power density is two times higher.

The heat-sink for a liquid cooling system is shown as well [30], where the CSPI is much higher compared with the air-cooling system. Here, it should be noted that the volume for the liquid-cooing is excluding external equipment such as pump, pipe and heat-exchanger. However, the thermal resistance is much smaller than the thermal resistance of the air-forced cooled heat sinks. For this reason, it is better suitable to improve the utilization of the power semiconductors.

For comparison, a thermal resistance of a power electronic module rated for 1 kA can be approximately 0.05 K/W. With (4), it can be demonstrated that the improved heat sink performance is enabling to increase the losses dissipated by the converter.

$$T_j = (R_{th,S-a} + R_{th,j-S}) \cdot P_{loss} \tag{4}$$

As an example, the thermal resistance from junction to heatsink $R_{th,j-S} = 0.05\ K/W$ and a design for a similar maximum junction temperature is assumed. In this case, the heat sink design 2 and 4 are compared and the losses can be increased by:

$$\frac{P_{loss}\left(R_{th,S-a} = 0.25K/W\right)}{P_{loss}\left(R_{th,S-a} = 0.1K/W\right)} = \frac{0.3\ K/W}{0.15\ K/W} = 2 \tag{5}$$

Therefore, 100 % more losses can be dissipated for the water-cooled heat sink than for the second design with the forced-air cooled heat sink. This improves the utilization of the power semiconductors, which is commonly limited by reliability requirements to a certain maximum junction temperature. An increase of the power semiconductor losses by 100% enables to increase the transferred current significantly. For the quantification, the power converter topology needs to be chosen and the semiconductors need to be selected. However, the increase of the current will be lower than 100%. This is affected by the squared dependence of the conduction losses on the current, whereas the switching losses are approximately proportional to the current.

Based on the CSPI and (4), it is also possible to get an estimation about the costs for a certain heat sink design. Thereby, a constant CSPI is assumed and the costs are assumed to be proportional to the volume of the heat sink. This is a particular good match for air cooled systems, because their design is dependent on the volume and weight of the heat sink. Consequently, it is obtained:

$$Costs_{cooling\_system} \sim V_{CS} = \frac{1}{CSPI \cdot R_{th,S-a}} = \frac{1}{CSPI \cdot \left(\frac{T_j}{P_{loss}} - R_{th,j-S}\right)} \quad (6)$$

Table 11: Comparison of the characteristics of different core materials for medium frequency transformers [31].

Magnetic material	Fe-based Amorphous	6.5 % Silicon steel	Nanocrystalline	Ferrite
Manufacturer	Metglas	JFE	Hitachi Metals	Ferroxcube
Material	2605SA1	10JNHF600	Finemet FT-3H	3C92
Bsat (T)	1.56	1.88	1.23	0.4
Rel. Permeability, μ (0.1T, 10 kHz)	10,000	2000	-	1500
Curie Temp. (°C)	395	700	570	280
Continuous operating temperature (°C)	150	150	120	120
Thermal conductivity (W/mK)	10	10	-	3.5-5
Specific heat capacity (J/CKg)	540	536	-	700-800
Density (g/cm3)	7.19	7.53	7.3	4.8

Electrical Resistivity (μΩ/m)	1.37	0.82	1.2	$5*10^6$
Lamination Thickness (mm)	0.025	0.1	0.018	Bulk
Core fill factor	0.83	0.9	0.82	Bulk
Magnetostriction (ppm)	27	0.1	0	0.6
Core loss @0.2T, 20kHz (W/Kg)	43	80	10	8

2.7.4. Impact of the medium frequency transformer on the efficiency

Magnetic material characteristics

In the ST design, the medium/high frequency transformer design is a critical bottleneck. The four materials, which are typically considered for the medium/high frequency transformer are Fe-based Amorphous, 6.5% Silicon Steel, Nanocristalline and Ferrite. **Table 11** describes the characteristics of the four magnetic materials, where green colour represents the best performance among four and red colour is the worst performance among four materials [31]. The continuous operation temperature for the transformer cores is comparable to the temperature of power semiconductors. However, for compact systems also liquate cooling systems for transformers can be adopted as it is already done for filter inductors in some commercial products.

Based on the table, the 6.5 % silicon steel material has the highest saturation flux density (1.88T), thermal conductivity (18.6W/mK) and operating temperature (150°C). Further, the magnetostriction is almost zero, resulting in a lower noise in audible range (16 – 20 kHz). However, the silicon steel has the thickest lamination, which causes higher nominal core losses (i.e. lower system efficiency). The Fe-based amorphous has the highest operating temperature (150°C) and shows a good compromise between the saturation flux density and the core loss, meaning the best performance of the saturation flux density with the moderate core loss. However, the high magnetostriction (27 ppm) limits the use of this material in the medium frequency range, because of noise. The nanocristalline features the lowest core losses but obtains a lower saturation flux density and operating temperature compared with the other materials. As it can be noticed, the performance of the nanocristalline is well balanced (i.e. the best overall performance), but this material is the most expensive one. Finally, the Ferrite has the strength in the high resistivity (5*106 μΩ/m), which allows not to suffer from additional eddy-current core losses due to fringing of the air-gap. This means that for large ripple ratios leading to an increase in gap size, the Ferrite core gap loss does not increase.

The considered magnetic materials are evaluated by the “area product deviation method”, introduced in [31], that includes the foil AC copper loss effects and the core loss due to air-gap. Thereby, a natural convection cooled inductor for a low ripple 40 kW boost converter is considered as a case study.

Figure 32 shows the influence of the operating frequency on the area product and loss, where the diamond marker is Fe-based amorphous, the square is 6.5 % Si Steel, the triangle is Nanocrystalline and the cross represents Ferrite material. As it can be seen in **Figure 32 (a)**, the increased frequency enables to reduce the area product, because the ripple current is reduced and in turn, the core losses can be reduced. The Ferrite is the largest inductor over the analysed

frequency range due to the low saturation flux density. The nanocrystalline and the Fe-based amorphous enable the smallest inductor size with the high saturation flux density. The 6.5 % Si steel has the high core loss, which results in the bigger size and highly frequency dependent core size. **Figure 32 (b)** shows that the 6.5 % Si steel has the highest loss and the Nanocrystalline has the lowest loss. Even though Ferrite is the material with the least core losses, the total loss is similar with the Fe-based amorphous due to the high copper loss of the Ferrite.

In **Figure 33**, the peak-to-peak ripple ratio (Ipk-pk/Idc) is varied from 0.125 to 2, when the frequency is fixed at 20 kHz. As shown in **Figure 33 (a)**, the area product of the Fe-based amorphous, 6.5 % Si steel and Nanocrystalline is increased for the laminate materials as the ripple ratio is increasing, whereas that of the Ferrite is decreased with higher ripple ratio. **Figure 33 (b)** shows the relation between the core loss and the ripple ratio. The core loss of the 6.5 % Si steel and the Fe-based amorphous is increased as the ripple ratio is increasing. The Nanocrystalline core loss is initially increased by the limited saturation flux density, but once that is limited by the specific power, the inductor loss is increased. On the other hand, the core loss of the Ferrite is decreased with increasing ripple ratio as it is limited by the saturation flux density, which leads to make the Ferrite competitive at high ripple ratio.

From the point of the isolation transformer design for the ST, a higher switching frequency would allow a reduction of the transformer for all core materials mentioned above. The influence of the ripple current shown in **Figure 33** shall be also applicable for the transformer if a ripple current ($I_{pk\text{-}pk}$) replaces the ripple ratio ($I_{pk\text{-}pk}/I_{dc}$) and the Ferrite is the best suitable material for the medium frequency transformer with a high current ripple.

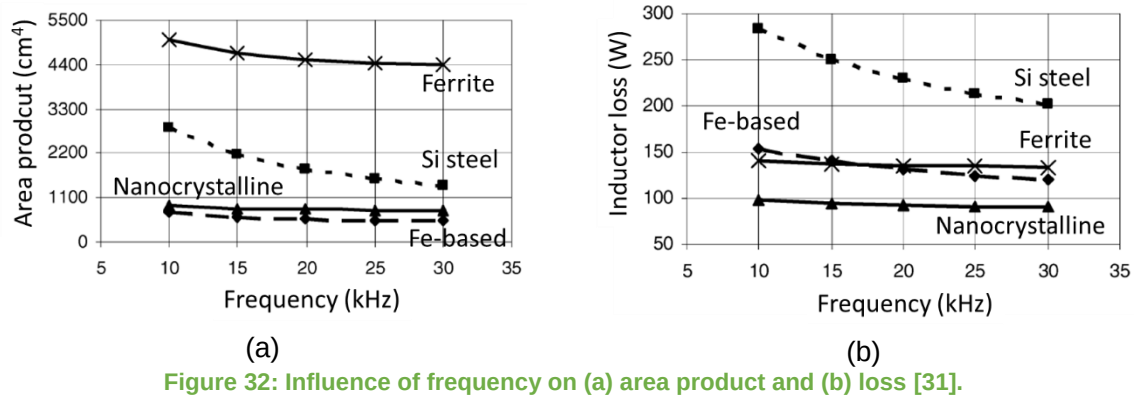


Figure 32: Influence of frequency on (a) area product and (b) loss [31].

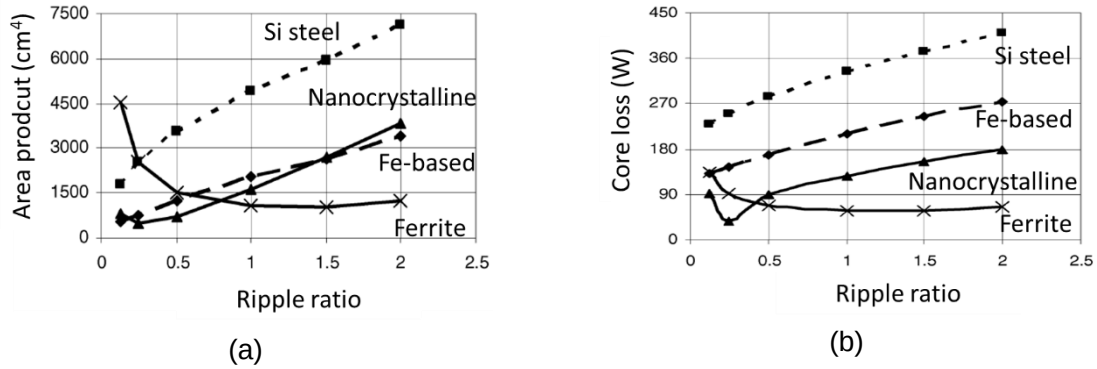


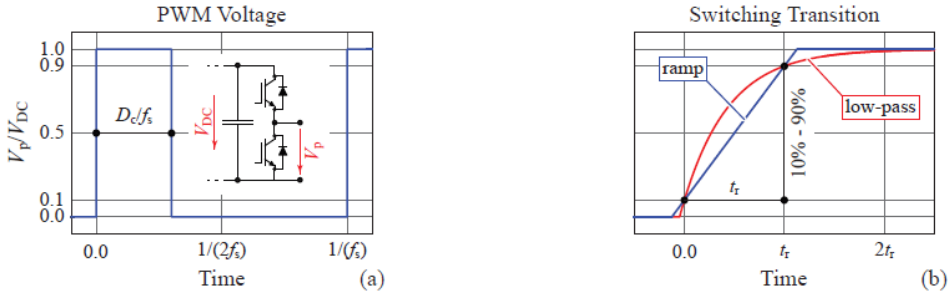
Figure 33: Influence of ripple ratio (Ipk-pk/Idc) on (a) area product and (b) core loss [31].

Dielectric losses in high voltage medium frequency application

The utilization of power semiconductors with high blocking voltage and high switching frequencies by power converters considerably increases the insulation stress of magnetic components (such as inductors and transformers), resulting in increased insulation failure rates. The insulation stress is related to the dielectric losses and in the following, it is evaluated by examining the dielectric loss density in accordance to [32].

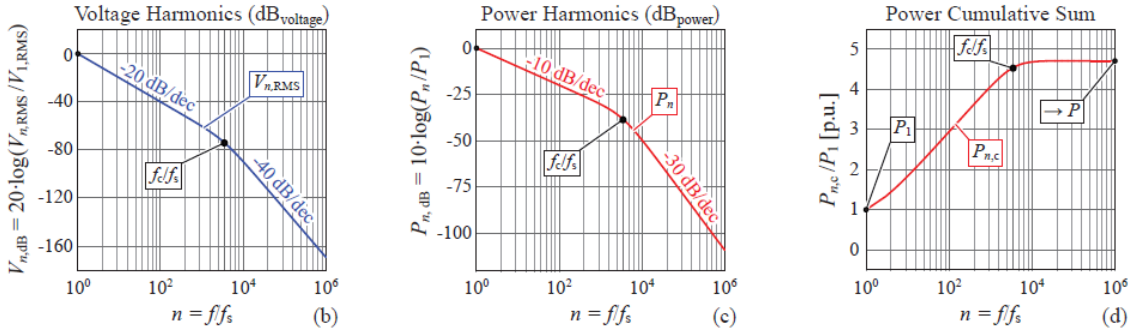
Dielectric loss with constant duty cycle in DC/DC converter:

In steady state, DC/DC converters generate PWM voltages with a constant duty cycle (**Figure 34 (a)**), which is usually 0.5 for isolated DC/DC converter. To evaluate the dielectric loss, the PWM voltages are modelled with the step response of a first order low-pass filter as shown in **Figure 34 (b)**.



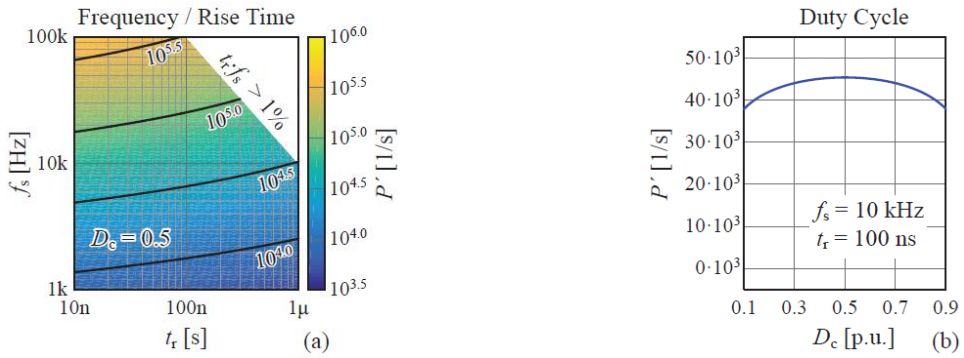
(a) (b)

Figure 34: PWM signal with a constant duty cycle. (b) Approximations of the switching transition: the ramp function and the step response of a first order low-pass filter [32].



(a) (b) (c)

Figure 35: Envelope of (a) the voltage harmonics, (b) the power losses harmonics and (c) cumulative sum of the power harmonics [32].



(a) (b)

Figure 36: Impact of (a) the switching frequency and rise time and (b) duty cycle to the dielectric loss [32].

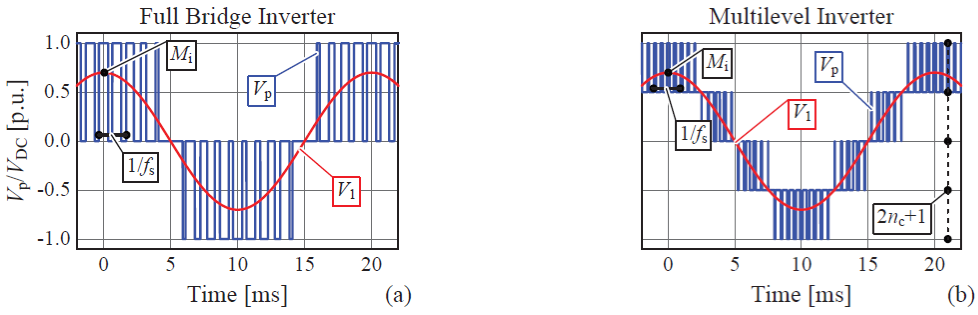
The voltage harmonics of the converter affects currents and therefore, the spectrum of the voltage, and the power needs to be analysed. For this purpose, the voltage harmonics, the losses spectral components and the cumulative sum of the losses are shown in **Figure 35 (a)**, **(b)** and **(c)**, respectively, where the horizontal axis is the harmonics order, *n*, and f_s is the switching frequency. The voltage and power harmonics are proportional to *1/n* for frequencies below the corner

frequency, f_c of the low-pass filter. Hence, the cumulative sum converges after the corner frequency, implying that shorter switching transition would lead to higher cumulative loss.

Figure 36 (a) shows the influence of the rise time and the switching frequency on the dielectric loss. As it can be seen, the switching frequency significantly affects the dielectric loss, whereas the impact of the rise time is logarithmically. Finally, the impact of the duty cycle is demonstrated to be minor as shown in **Figure 36 (b)**.

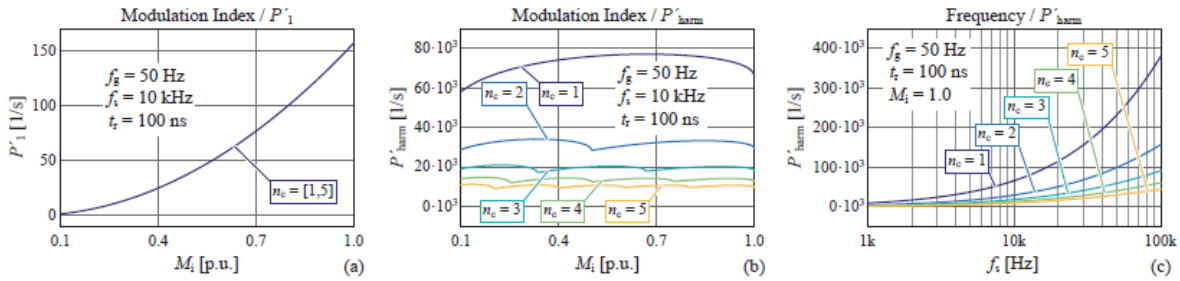
Dielectric loss with sinusoidal duty cycle in DC/AC inverter:

Similar to the DC/DC converter, it is also important to evaluate the insulation stress of AC side magnetic components, which is mixed frequency stress from the grid-frequency to switching frequency. **Figure 37** shows the PWM voltages produced by the typical 2-level inverter (**Figure 37 (a)**) and the multilevel cascaded H-bridge inverter (**Figure 37 (b)**), where n_c is the number of cells. To derive the dielectric loss from these PWM voltages, the local averaging approach is employed.



(a) (b)

Figure 37: PWM voltages of (a) 2-level inverter and (b) multilevel cascaded H-bridge inverter [32].



(a) (b) (c)

Figure 38: Impact of (a) the modulation index of the fundamental component and (b) the higher harmonics and (a) the switching frequency on the dielectric loss [32].

Table 12: Grid voltages and power rating of the ST.

LV AC voltage	0.4 kV (rms)
MV AC voltage	11 kV (rms)
ST power	500 kVA

The influence of the modulation index is shown in **Figure 38 (a)** and **(b)** on the dielectric loss. As shown in **Figure 38 (a)**, the impact of the fundamental frequency is proportional to the square of the modulation index and it is independent on the number of levels, whereas the impact of the higher order harmonics is not strongly affected by the modulation index. Comparing the impact of the fundamental and the higher order harmonics, the dielectric loss by the higher order harmonics is much higher. Furthermore, the number of levels affects the dielectric loss by the high order harmonics, where it is oscillated n_c times and reduced as n_c is increasing. Finally, a higher switching frequency generates a higher dielectric loss as shown in **Figure 38 (c)** and it is also shown that the higher number of levels can significantly reduce the dielectric loss. This is due to the reduction of voltage steps by the multilevel PWM voltage and highlights advantages of multilevel inverter in medium voltage applications.

2.8. Sizing of the power semiconductors

The power semiconductors need to be sized for the blocking voltage and the rated power of the system, taking into account the root means square (rms) value of the device current as well as the thermal design. For the considered LV Engine, the power rating and the grid voltages are shown in **Table 12**. In the following, first the impact of the temperature on the maximum current of the power semiconductors is discussed. The blocking voltage for the system will be derived and the current rating for the system, assuming the application of specific standards, is derived. At the end of the subsection, a discussion about emergency current ratings is made.

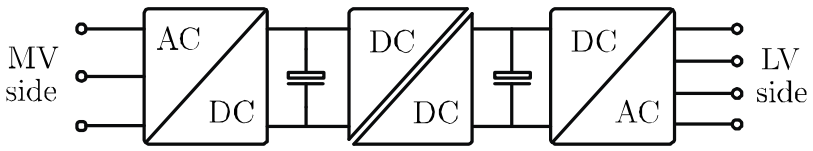


Figure 39: Three stages ST architecture.

2.8.1. Impact of the junction temperature on maximum power semiconductor current

The maximum current, which a power semiconductor can conduct is related to its ambient conditions and its junction temperature. Therefore, the current rating of a device is meaningless without reference to the operating temperature. A single value for the current rating can only be used to compare devices with a similar current and voltage rating, but it does not apply outside the specified setpoint. As an example, for a MOSFET, the maximum continuous drain current I_D can be describe with the following equation:

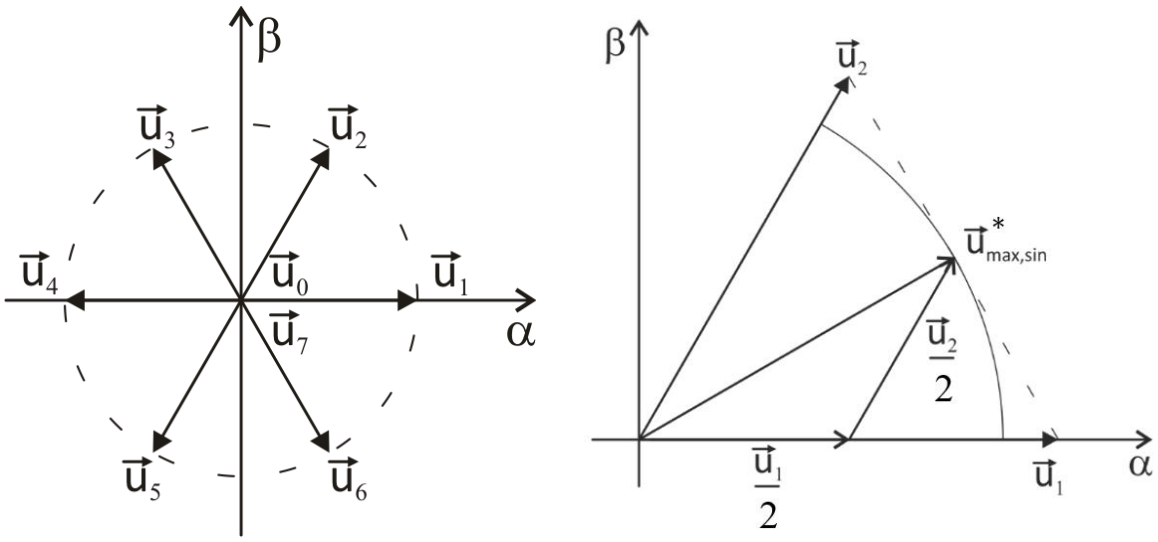
$$I_D = \sqrt{\frac{T_{j,max} - T_c}{R_{DS(on)} \cdot R_{th,(JC)}}} \tag{7}$$

Thereby, $T_{j,max}$ is the maximum allowed junction temperature (e.g. 175°C), T_c is the case temperature of the power semiconductor, $R_{DS(on)}$ is the on-state resistance and $R_{th,(JC)}$ is the thermal resistance between junction and case. In the ac-stages of the ST, the current will not be a continuous drain current, but it will be sinusoidal and during a fundamental period of the grid. Multiple power semiconductors will conduct the current and share the stress. As an example for the two level voltage source converter, the current of one phase is conducted through four power semiconductors (two switches and two diodes).

Physically, the maximum junction temperature is limiting the maximum losses and if each device of a converter stays within these maximum losses, the converter can maximize its current. To analyze this potential, the losses are split into conduction losses and switching losses, whereby the latter ones can be manipulated by the control of the system by changing the switching frequency. This may be a solution to increase the maximum short circuit current of a converter without destroying the switches. The cost for this control action is a higher output current ripple, which is not accepted during the fault-free operation, but may be accepted during faults.

2.8.2 Impact of grid conditions on the sizing of the power semiconductors

LV DC link rating (worst-case consideration):



(a) (b)

Figure 40: (a) Space vectors of a 2 level VSC and (b) maximum sinusoidal converter output voltage of the 2 level VSC.

For obtaining the minimum DC-link rating of the devices, the operation of the converter needs to be considered. In the following, this is examined for a LV stage of a three-stage ST architecture as shown in **Figure 39.** In the LV stage, a 2 level voltage VSC with its 8 space vectors is considered as shown in **Figure 40 (a)**. The space vectors $\underrightarrow{u}_1$ ... $\underrightarrow{u}_6$ are active vectors and the vectors $\underrightarrow{u}_0$ and $\underrightarrow{u}_7$ are zero voltage vectors. The output voltage of the converter is synthesized by a combination of 2 active and 1 or 2 zero voltage vectors in such a way that the average output voltage generates the reference voltage. As it can be seen in **Figure 40 (b)**, the maximum sinusoidal output voltage $\underrightarrow{u}_{max,sin}$ is lower than the magnitude of the space vector $\underrightarrow{u}_1$.

This maximum sinusoidal output voltage needs to be higher than the maximum voltage, which is required to be generated at the converter output and can be expressed with

$$\underrightarrow{u}_{max,sin} = \frac{\sqrt{3}}{2} \cdot |\underrightarrow{u}_1| \approx 1.15 \frac{V_{dc}}{2} \tag{8}$$

In this equation, V_{dc} is the DC-link voltage of the 2 level VSC. This DC-link voltage needs to be sized in order to be able to compensate to enable a power injection into the grid and additional voltage drops, like the voltage drop on the output filter of the converter $\hat{V}_{filter}$ needs to be considered. In addition, possible disturbances $\Delta\hat{V}_{Disturbance}$, which are required to ride through may also affect the required minimum DC-link voltage.

Consequently, for a nominal peak grid voltage $\hat{V}_{grid,rated}$ the minimum voltage to fulfil this requirement can be expressed with the following equation:

$$\hat{V}_{DC,min} = \hat{V}_{grid,rated} + \hat{V}_{filter} + \Delta\hat{V}_{Disturbance} \tag{8}$$

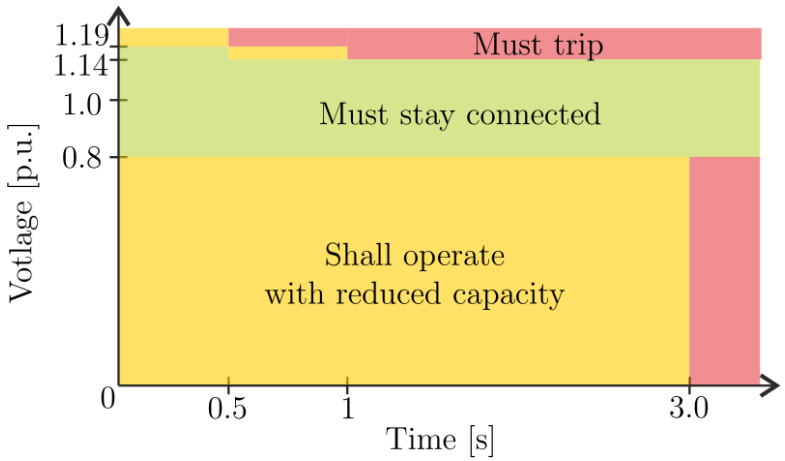


Figure 41: Requirements for LV converters according to G99.

In the equation, the rated peak grid voltage is:

$$\hat{V}_{grid,rated} = 566\,V \tag{9}$$

And the voltage drop on the output filter is approximated to be ~5 % of the grid voltage, which is a conservative estimation:

$$\hat{V}_{filter} = \hat{V}_{grid,rated} \cdot 0.05 = 28\,V \tag{10}$$

The disturbances $\Delta\hat{V}_{Disturbance}$, which can occur in the grid are not know, but for certain disturbances, the regulations require the system to trip and to disconnect. Consequently, the tripping and disconnecting needs to be only considered for the cases, in which the ST needs to

continue to operate. To the current state, there are no specific standards for the ST and therefore, the guidelines for generators defined in the British Codes G99 are used. For the LV-side converter, this is shown in **Figure 41**.

This code is used in the following, to evaluate the impact on the minimum grid voltage. As it can be seen in **Figure 41**, the maximum voltage, which may needs to be ride through is 119 % of the rated voltage, which corresponds to a voltage disturbance of:

$$\Delta\hat{V}_{Disturbance} = \hat{V}_{grid,rated} \cdot 0.3 = 107\,V \tag{11}$$

Under full load, and consequently the full voltage drop on the filter, this may results in a maximum DC-link voltage of:

$$V_{DC,min} = \hat{V}_{grid,rated} \cdot 1.35 = 701\,V \tag{12}$$

This voltage may only be hold for 0.5 s, before the system is required to trip and corresponds to the minimum DC-link voltage of the LV-side converter.

As a result form the considerations, the minimum DC-link voltage is recommended to be considered for the case of grid forming operation and therefore $V_{DC,min} = 700\,V$. This enables to use standard 1.2 kV power semiconductors, which are commercially available in the market. Their maximum DC-link voltage is recommended to be below $V_{DC,max} = 800\,V$. Therefore, the DC-link voltage recommended between $V_{DC} = 700 \ldots 800\,V$.

MV DC link rating (worst case consideration):

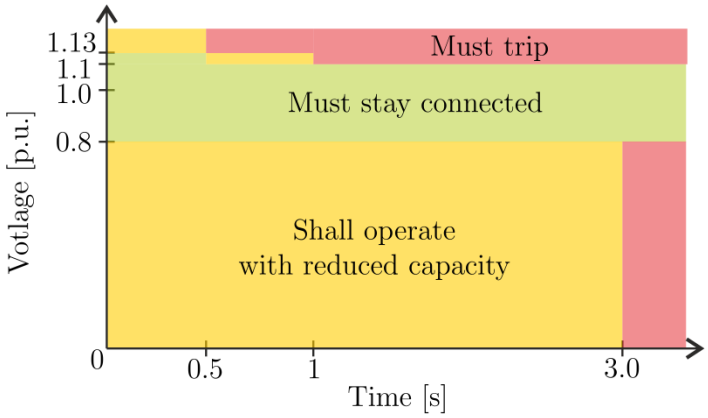


Figure 42: Requirements for MV converter according to G99.

Similar to the considerations in the LV grid connected converter, the MV-side connected converter is investigated with respect to the British Codes G99, which is shown in **Figure 42**. The nominal peak grid voltage of the MV-side is

$$\hat{V}_{grid,rated} = 15.556\,kV \tag{13}$$

Similar to the LV-side, a worst case assumption for the voltage drop on the filter is assumed:

$$\hat{V}_{filter} = \hat{V}_{grid,rated} \cdot 0.05 = 778\,V \tag{14}$$

As it is shown in **Figure 42**, the maximum voltage required to ride through is 113 % of the grid voltage for $0.5\ s$, which results in the maximum

$$\Delta\hat{V}_{Disturbance} = \hat{V}_{grid,rated} \cdot 0.13 = 2.02\ \mathrm{k}V \tag{15}$$

Consequently, the minimum DC-link voltage (between line-to-line) is:

$$V_{DC,min} = \hat{V}_{grid,rated} \cdot 1.18 = 18.36\,kV \tag{16}$$

This is a relatively high voltage and to the knowledge of the authors, there are no commercially available power semiconductors, which can block this voltage. Therefore, it is necessary to use multilevel converters, which are available in various topologies. Remarkably, the analysis is done for a 2 level VSC and other for topologies, this voltage requirement may differ because of a connection in star or in delta.

For the minimum DC-link voltage sizing, it is recommended to design the system for 118 % of the rated grid voltage. This requires to use a multilevel converter for being able to use commercially available power semiconductors. The detailed design is dependent on the selected converter topology and on the number of building blocks. Here, also a certain redundancy may be considered for fault tolerance. Important in this context is the considered hot/cold reserve of series connected building blocks in the system. Thereby the hot reserve refers to the activated reserve, whereas cold reserve refers to deactivated reserve modules.

Sizing of the semiconductors in consideration of the norms:

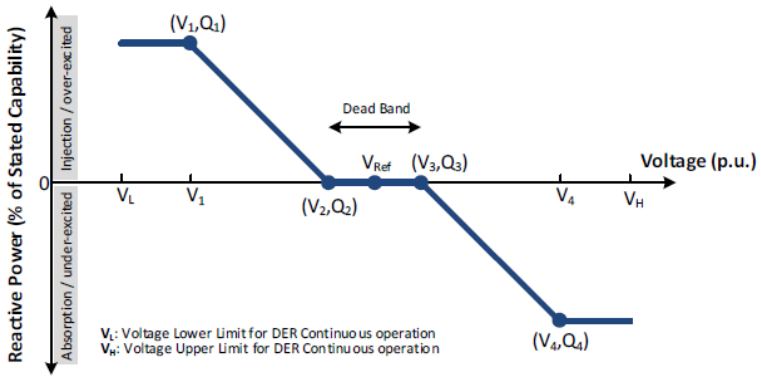


Figure 43: Reactive power control: (IEEE Std. 1547, required for MV side).

For the design of the power semiconductors, there are several influencing factors, such as the power absorbed/injected into the grid, the power factor and the voltage variations. In the following, different operation conditions and their impact on the power semiconductor loading is investigated. As the starting point for the analysis, the nominal grid current I_{line} under consideration of the power of the ST S is derived in dependence of the grid voltage V_{line} and the power factor $\cos(\varphi)$:

$$I_{line} = \frac{S}{\sqrt{3} \cdot V_{line} \cdot \cos(\varphi)} = 721.7\ A\ (rms) \tag{17}$$

For the sizing of the power semiconductors, the rms current of the switches is used. Thereby, it needs to be considered if the active switches (IGBTs, MOSFETs) or the diodes are conducting the current. The result is dependent on the topology and the modulation of the converter. As an example, here it is described for the active switch in a 2 level voltage source converter:

$$I_{switch,rms} = \sqrt{\left(\frac{1}{8} + \frac{m \cdot \cos(\varphi)}{3\pi}\right) \cdot 2 \cdot (I_{line})^2} \tag{18}$$

As it can be seen, the rms current is dependent on the power factor, the magnitude of the line current and the modulation index m. The modulation index itself is dependent on the DC-link voltage and the output voltage of the converter:

$$m = \frac{2 \cdot \hat{V}_{line-0}}{V_{dc}} \tag{19}$$

According to IEEE Std. 1547, the ST systems are required to support the grid with reactive power injection. Consequently, the power factor may vary in the whole operation range. In **Figure 43**, this is shown for the MV-side converter.

The line voltage variations thereby influence the rms current of the switches and the constant power behaviour in the grid feeding operation affect a variation of the output current. For assuming the worst case, the extreme conditions are analysed along with their impact on the rms current of the power semiconductors:

First, the modulation index is assumed to be *m=1* and $\cos(\varphi)$, which is the worst case for active switches and the least stressing condition for the diodes. The rms current results with (18) in

$$I_{switch,rms} = 0.58\, I_{line} \tag{20}$$

For pure reactive current injection, $\cos(\varphi) = 0$, it results in :

$$I_{switch,rms} = 0.35\, I_{line} \tag{21}$$

And for reversing power flow assuming m=-1 and $\cos(\varphi) = 0$ it results in:

$$I_{switch,rms} = 0.3\, I_{line} \tag{22}$$

This shows that the difference between the rms current of the switches can be up to 2 times between different operation conditions. Consequently, the stress is highly dependent on the power factor and without prior knowledge about the expected operating conditions, it is required to size the power converter for the whole operating range.

As it was shown in (17), the grid voltage is influencing the line current and therefore, the duration and the magnitude of voltage dips impact the power semiconductor stress. This is of importance, because the ST may behave similar to a constant power load in the other AC grid, which means a voltage dip in the grid is affecting a rise of the current. The mathematical expression of voltage drip to $V_{line,ST}' = aV_{line,ST}$ and the impact on the line current of the switches is described as:

$$I'_{line} = \frac{S_{ST}}{\sqrt{3} \cdot V_{line,ST'} \cdot \cos(\varphi)} = \frac{I_{line}}{a} \tag{23}$$

From this, the rms current of the switches results in:

$$I_{switch,rms}{}' = \frac{1}{a}\sqrt{\left(\frac{1}{8} + \frac{m' \cdot \cos(\varphi)}{3\pi}\right) \cdot 2 \cdot (I_{line})^2} \tag{24}$$

In both AC converter stages, the minimum grid voltage to stay connected is $V = 0.8 \cdot V_{line,ST}$. This results in

$$I'_{switch,rms}(V = 0.8 \cdot V_{line,ST}) = 1.17 \cdot I_{switch,rms}(V = V_{line,ST}) \tag{25}$$

This is an increase by 1.17, which also needs to be considered in the design. Below this voltage limit, the converter may operate for $2.5\, s$ with even lower voltage (e.g. during startup or short transients).

As a result from the analysis, there is in general an impact from the norms on the design of the converter. Without additional consideration of the operation conditions in dependence on the trail side, it is recommended to design the AC converters for the whole range of power factors (-1…1). It is recommended to take the results from the voltage dips into account in the sizing of the current rating for the converters connected to the AC sides.

The current rating of the converters needs to have a sufficient margin to ride through faults, which are described in the considered norms. In addition, the cooling system needs to be designed in order to be capable of removing these additional losses. Remarkably, the conduction losses have a quadratic dependence on the rms current.

In grid feeding operation, both grids may experience an increase of the rms current for the switches by 17%.

2.8.3. Impact of fault currents on system design

In the following, considerations will be made about the sizing of the devices in the ST taking into account possible fault currents in the grid. The protection of the grid is organized in a hierarchical way, so that the breaker/fuse closest to the fault is tripping, whereas the rest of the grid can continue to operate. To realize this, the sensitivity of the protection needs to ensure that the protection closest to the fault trips first. Therefore, a fault current with sufficient magnitude needs to be injected. This fault current needs to be provided by the ST and therefore, its components need to be sized to be able to provide it. Remarkably, in contrast to the conventional transformer, the voltage of the ST is controlled and the derivation of the fault current more complex. The ST enables to maintain the grid voltage by increasing the output current of the ST. This is possible to a certain extent until the control limits the current to a maximum to prevent destruction of the system (usually thermal destruction).

Of course, a fault close to the ST will affect a high fault current and will affect a grid voltage sag along with an impact on the DC-link voltage of the converter. In this case, the ST will have to disconnect and there is no opportunity to continue to operate. In order to analyse the required current carrying capability, the protection with fuses is considered in the following. The typical characteristics of a fuse are shown in **Figure 44**. In addition to the boundaries for which the fuse is tripping, the rated current of the converter (considering a rating for 500 kVA ST in the LV grid) is highlighted in blue and the thermal constraint of the converter rating is sketched in red. As it can be seen, the current, which affects a fuse to trip is time dependent and multiple times higher than its rated current.

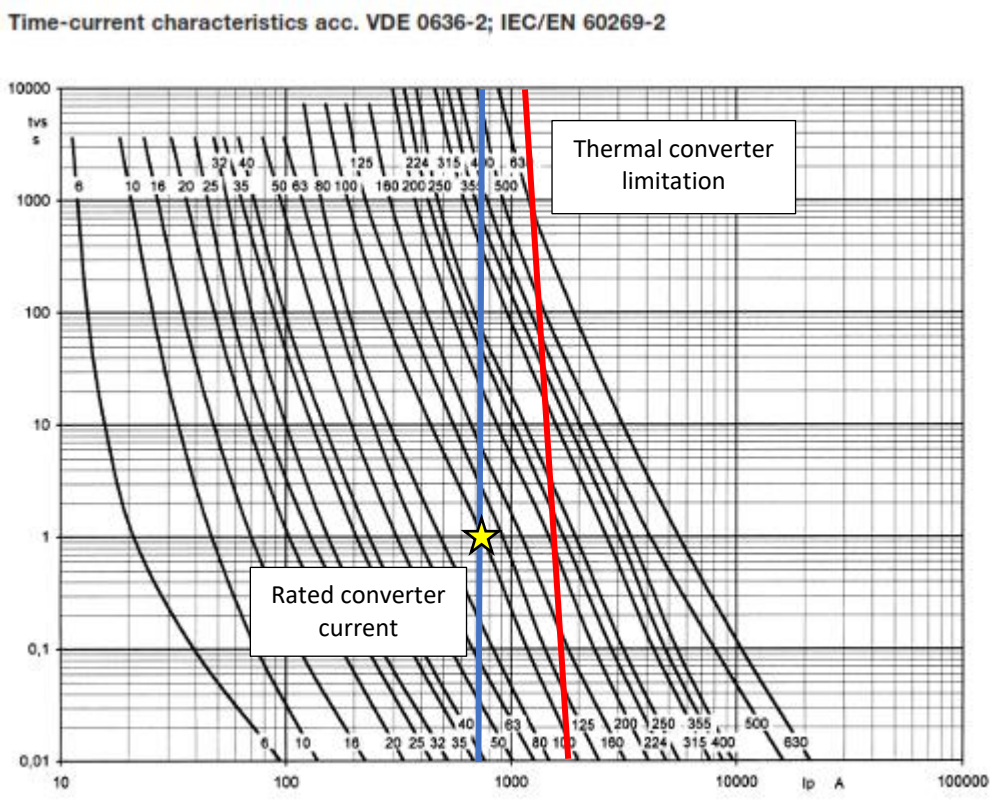


Figure 44: Typical time-current characteristics of fuses according to IEC/EN 60269-2 with indication of the rated converter current and sketched thermal converter limitation.

As an example, the highest rated fuse in the feeder is rated for 100 A and the fuse is expected to trip after 1 s. This results in a required fault current of 700 A, which is similar to the rated current (marked with the yellow star in **Figure 44**). A longer time to trip requires a lower current and a short time an even higher fault current to trip the fuse.

As an additional challenge, the fault current needs to be provided in addition to the current supplied to the other loads and therefore, the capability to provide a certain fault current also depends on the loading of the ST. For the example given before and full load operation during the fault, the ST is requested to operate with 2 times the rated current for 1 s. This is a challenge for the devices and requires the system to be designed accordingly. For minimizing the overdesign for the fuses in the feeder, the actual trial sites should be considered in the design and the fault current, which is needed has to be evaluated.

For a minimization of the overdesign, the overload capability of the power devices in the ST can also be considered. Usually, the most stringent limitation of devices in the ST is the maximum current, which is dependent on the temperature of the power semiconductors. For obtaining a desired margin, this can be considered in the design of the system and in particular the cooling system. As an opportunity to store energy in the system without additional batteries, the DC-link capacitance can be increased and thereby energy from the DC-link can be used to supply the fault current. However, this can only contribute to short transients and the thermal constraints of the power semiconductors still need to be considered.

3. Software for the Smart Transformer

This section reviews the basic control schemes of the Smart Transforms and it specifies the software requirements for the ST. The ST control in the stationary and rotating reference frames are reviewed and the controller design for grid forming (voltage control) and the grid feeding (power control) are introduced. The change between voltage control and power control is addressed and communication requirements as well as controller implementation are discussed.

3.1. Controller design

The control variables of the AC-stages of the ST are the power and the grid voltage. The reactive power and the voltage cannot be controlled independently. The controller of the voltage and the power control can be implemented in different coordinate systems, which result in different designs. In the following sections, the possible control variables in case of different ST architectures, the coordinate transformation, the controller design and the fundamental synchronization mechanisms are introduced.

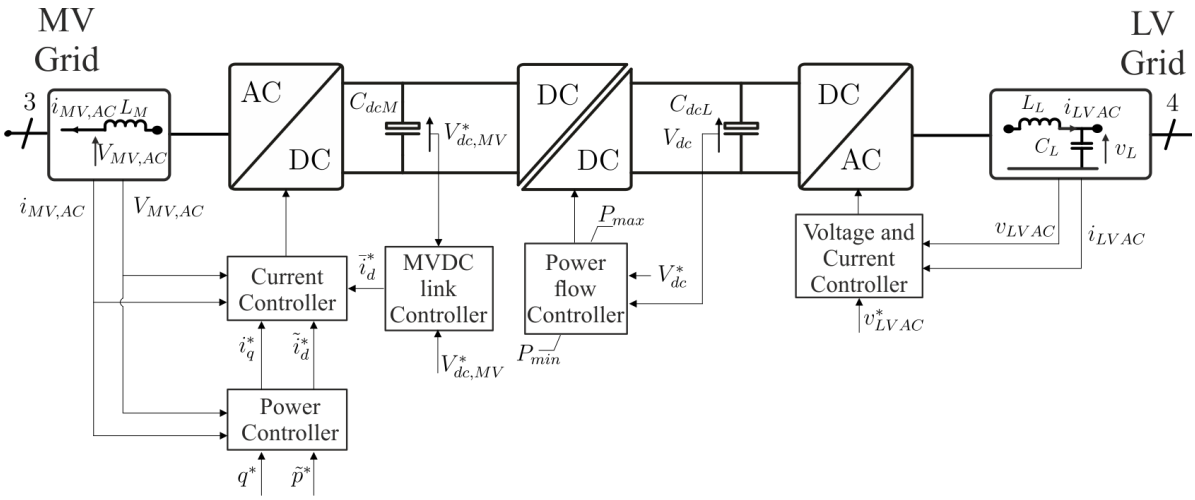


Figure 45: Control diagram of a three-stage ST architecture.

3.1.1. Control of various ST architectures

A general control structure for a three-stage ST is shown in **Figure 45**. As it can be seen, the controllers of the AC-grid-side converters define either the voltage or the apparent power exchanged with the grid. The DC/DC converter is required to control the active power flow within the ST for ensuring constant LV DC-link voltage. As a degree of freedom, the voltage references (magnitude, frequency, and phase) of the AC-grids (MVAC-grid and LVAC-grid) in voltage control can be set by an external reference signal. Alternatively, if both AC-grids operate in power control mode, the power reference can be set externally.

Based on this general control diagram, the controller design for different ST architectures is addressed. Suitable control variables are assigned for different architectures and the control objectives are highlighted. This is done for a single-stage ST, two-stages ST and a three-stages ST.

a) Single-stage ST

In the configuration of the single stage ST, it needs to be highlighted that the voltages on both sides are coupled and no control action can be performed without impacting the other grid side. Consequently, the control capability is limited in terms of reactive power control, harmonic filtering and disturbance rejection. The control variables for the single-stage ST are defined in **Table 13**.

Table 13: Control variables for the different stages in a single stage ST architecture.

Mode 1 (MV: grid feeding / LV: grid forming)	• LV grid amplitude • LV grid frequency
Mode 2 (MV: grid forming / LV: grid feeding)	• MV grid amplitude • MV grid frequency

b) Two-stages ST

Table 14: Control variables for the different stages in a two-stage ST architecture.

	MV stage	LVDC-link	LV stage
Mode 1 (MV: grid feeding / LV grid forming)	• Active/reactive power • LV DC-link voltage • PLL (MV grid)	-	• LV grid amplitude • LV grid frequency
Mode 2 (MV: grid forming / LV: grid feeding)	• MV grid amplitude • MV grid frequency	-	• Active/reactive power • LV DC-link voltage • PLL (LV grid)

The two-stage ST has the capability to decouple the power flow between the two grids to a certain extent. Depending on the storage of the DC-link/s, it is possible to control active power and reactive power individually. Moreover, it is possible to connect a DC-grid to a potentially available DC-link, which needs to be controlled as well. As a problem from this configuration, in mode 1, the MV needs to control the DC-link voltage and in mode 2, the LV stage needs to control the DC-link voltage. This results in a challenge to change the control objective, without disturbing the normal operation. The control variables for the two-stage ST are defined in **Table 14**.

c) Three-stages ST

Similar to the two-stage ST, the three-stage ST enables to control the active and reactive power in both AC-grids. In this configuration, the control objectives of the MV stage and the LV stage are similar to the control objectives of the two-stage ST. As an additional challenge, the isolation stage needs to control either the LVDC-link (in mode 1) or the MVDC-link (in mode 2). This requires changing the control objective as it was discussed for the two-stage ST. For the control of the three-stage ST, the dynamics of the different stages need to be considered and suitable feedforwards may be added to increase the dynamic performances of the stages. For this purpose, a feedforward of the power may be required in one or more stages. Particularly, the isolation stage with its non-linear behaviour may require this feedforward of the power. However, this results in an additional challenge, if the operation is changed between power control and voltage control. The control variables for the single-stage ST are defined in **Table 15**.

In the following, the LV Engine schemes are considered and the different possible control objectives are shown. This is intending to provide an overview on the control objectives and to demonstrate the impact of the grid configuration. Thereby, the status of the Normal Open Point (NOP) changes the LV grid configuration between a radial grid and a meshed grid.

Table 15: Control variables for the different stages in a three-stage ST architecture.

	MV stage	MVDC/LV DC stage	LV stage
Mode 1 (MV: grid feeding / LV: grid forming)	• Active/reactive power • MV DC-link voltage • PLL (MV grid)	• LV DC-link voltage	• LV grid amplitude • LV grid frequency
Mode 2 (MV: grid forming / LV: grid feeding)	• MV grid amplitude • MV grid frequency	• MV/LV DC-link voltage	• LV grid amplitude • LV grid frequency • PLL (LV grid)

Table 16: Control mode in dependence of the NOP status in the different LV Engine schemes.

LV Engine schemes	NOP status	Operation mode of the LV side converter
1	NOP Closed	Grid feeding mode
	NOP Open	Grid forming mode
2	NOP1 closed / NOP2 closed	Grid feeding mode
	NOP1 closed / NOP2 open	Grid feeding mode
	NOP1 open / NOP2 closed	Grid feeding mode
	NOP1 open / NOP2 open	Grid forming mode
3	NOP1 closed / NOP2 closed	ST 1,2 :Grid feeding mode
	NOP1 closed / NOP2 open	ST1: Grid forming mode ST2: Grid feeding mode
		ST1: Grid feeding mode ST2: Grid forming mode
	NOP1 open / NOP2 closed	ST1: Grid feeding mode ST2: Grid forming mode
	NOP1 open / NOP2 open	ST1, 2: Grid forming mode

Table 17: Control variables in dependence of the operation modes of the ST.

LV Engine schemes	Operation mode	Control loop	Control variables
1,2,3	Grid feeding mode	Active/reactive power	I_d / I_q
		DC-link voltage	V_{dc}
		PLL	θ
	Grid forming mode	Amplitude/frequency of ST output voltage	$\|V_g\|$ / f_g
4	-	LVDC voltage	$V_{dc,lv}$
5	-	LVDC voltage	$V_{dc,lv}$
	Grid feeding mode	Active/reactive power	I_d / I_q
		DC-link voltage	V_{dc}
		PLL	θ
	Grid forming mode	Amplitude/frequency of ST output voltage	$\|V_g\|$ / f_g

The resulting required control loops and control variables for the different LV Engine schemes and NOPs are summarized in **Table 16**.

Table 17 defines the control variables for the different LV Engine schemes for the grid feeding and the grid forming operation.

3.1.2. Coordinate transformations

a) Transformation from stationary reference frame into the synchronous reference frame

In general a three phase system is represented in abc-coordinates, whereas each of the indexes a,b and c is representing one phase. Thereby, *f* represents either the voltage or the current (f_a, f_b and f_c). This can be transformed into the stationary frame (αβ0), represented by (*26*).

$$\begin{bmatrix} f_\alpha \\ f_\beta \\ f_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2}{3}\pi\right) & \cos\left(\theta + \frac{2}{3}\pi\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2}{3}\pi\right) & -\sin\left(\theta + \frac{2}{3}\pi\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \cdot \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \quad (26)$$

where θ is the phase displacement between the a-axis and α-axis. An advantage of adopting a stationary reference frame in a three-phase three-wire system is the potential reduction of the system's order to two. This is possible because of $f_0 = 0$ and results in a simplification of the controller design. However, in a three phase four wire system, all three phases need to be controlled and $f_0 \neq 0$. The relation between the representation in the two reference frames is shown in **Figure 4**.

As it can be seen, f_α and f_β have a phase difference of 90°. For the sake of simplicity, the phase displacement θ is fixed at 0°, which implies that the a-axis and α-axis are in phase. This leads to the commonly applied equation in (*27*).

$$\begin{bmatrix} f_\alpha \\ f_\beta \\ f_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \cdot \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \quad (27)$$

Similarly, the variables in the stationary frame can be transformed back to the *abc* frame by (*28*).

$$\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \cdot \begin{bmatrix} f_\alpha \\ f_\beta \\ f_0 \end{bmatrix} \quad (28)$$

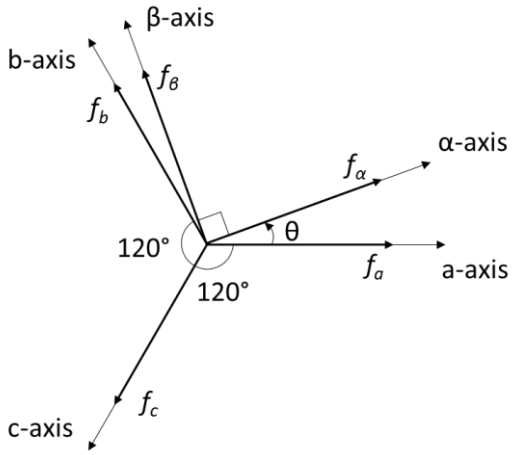


Figure 46: Variables in abc frame and stationary reference frame.

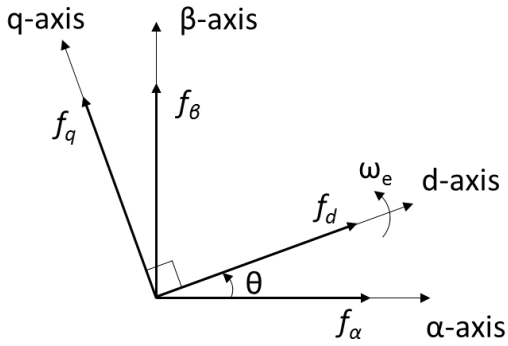


Figure 47: Variables in stationary reference frame and synchronous reference frame.

The components of the current vector in the stationary reference frame are still sinusoidal, which is a shortcoming, if a commonly used PI-controller is applied for the control of the current. For overcoming this, a rotating coordinate system is introduced, referring to the synchronous reference frame. The stationary frame *αβ0* can be transformed to the synchronous frame *dq0* that rotates at the synchronous speed ω_e. For grid connected applications, the synchronous speed is the angular speed of the grid voltage (i.e. $\omega_e=2\pi\cdot 50\cdot t$) and therefore, the quantities are becoming DC-quantities. Consequently, PI controllers can be used to control quantities in the synchronous reference frame. The two reference systems are visualized in **Figure 47**.

The transformation from the stationary reference frame into the synchronous reference frame is described with (*29*),

$$\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 0 \\ -\sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} f_\alpha \\ f_\beta \\ f_0 \end{bmatrix} \tag{29}$$

where $\theta = \int_0^t \omega_e(\tau)d\tau + \theta(0)$.

b) Control in the synchronous frame and the stationary frame

As stated before, the control of AC quantities can be performed in either the synchronous reference frame or the stationary reference frame. Remarkably, all control objectives can be achieved in both reference frames and there is no clear advantage of one or the other. The control block diagram for the ST in the synchronous reference frame is shown in **Figure 48**. To realize this controller, the variables in the *abc* frame are transformed into the rotating reference frame (*dq* frame) by using the angular speed of the variables in the *abc* frame. For the estimation of the angular speed of the grid voltage, a Phase Locked Loop (PLL) is employed, which will be introduced in the next subsection. The reference signals in the rotating reference frame are compared with the sensed signals and fed to the respective Proportional Integral (PI) controller. Remarkably, the variables in the synchronous frame are direct components.

The PI controller is not suited for controlling AC quantities even if a feed-forward term is added [33]-[34] and it shall be implemented only in a rotating dq-frame.

Advantageous for the PI-control in dq is the capability to directly control the active and reactive power by controlling the d-component and the q-component, respectively. Remarkably, a variation

of the output frequency is no concern, if the control is implemented in the synchronous reference frame.

For the harmonic elimination, additional PI-controllers in other rotating reference frames with other angular frequencies (e.g.250 Hz or 350 Hz) can be added or Proportional Resonant (PR) controllers can be put in parallel to the PI-controller [35].

The control block diagram for the stationary reference frame is shown in **Figure 49**. The controller does not need the αβ/dq transformation, which implies that the angular speed does not need to be estimated. The information about the angular frequency of the grid is included in the Proportional Resonance (PR) controller. The PR controller is able to eliminate a steady state amplitude error and phase errors, because it obtains a high gain at the resonance frequency. In addition, the low-order harmonics elimination can be combined with the fundamental current control by implementing more PR-controllers in parallel to the PR-controller for the fundamental frequency [36]. However, an exact frequency information is required to tune parameters of the PR controller.. According to the British Distribution Code G99, the generators require to stay grid-connected for a frequency range of 47-52 Hz and therefore, the control of the ST needs to be able to control the current/voltage within this frequency range. As a disadvantage of the control in the stationary reference frame, direct control of the active and reactive power is not possible and for this purpose, a PLL may be installed for reference generation. Consequently, it is expected that a PLL is required independently from the chosen reference.

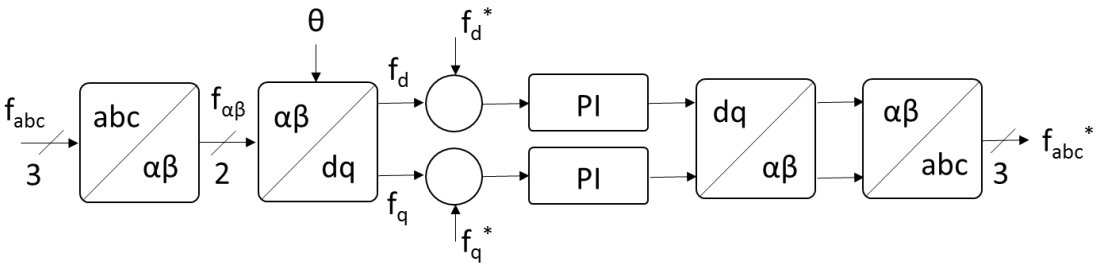


Figure 48: Typical control block in the synchronous frame.

3.1.3. Grid synchronization (PLL)

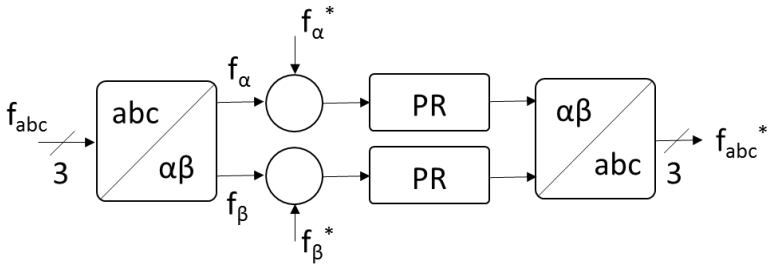


Figure 49: Schematic control block in the stationary frame.

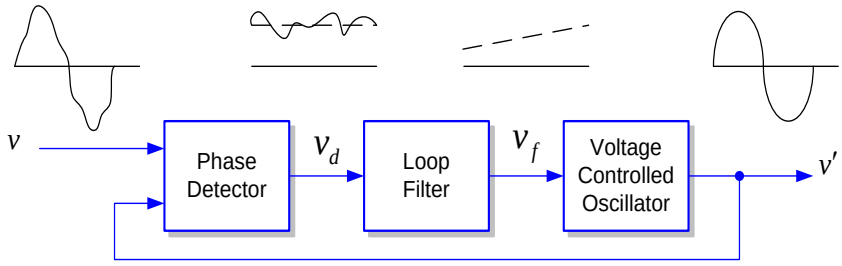


Figure 50: Basic structure of a PLL.

A PLL is a closed loop system for the detection of the grid angle. Potentially a frequency locked loop (FLL) is employed additionally for the detection of the angular grid frequency. The basic structure of a PLL is shown in **Figure 50** and it generally consists of three fundamental blocks, which are the phase detector, the Loop Filter (LF) and the Voltage Controlled Oscillator (VCO). The PD generates an output signal proportional to the phase difference between its two input signals. Depending on the type of PD, high frequency AC components (affected by high frequency

harmonics etc.) appear together in the output signal. The LF (Low-pass Filter, e.g. a PI) filters out the high frequency AC components from the PD output. The VCO generates an AC signal at its output, whose frequency varies in dependence of the input voltage.

a) Single-Phase PLLs

The Synchronous Reference Frame (SRF) PLL is widely used technique to extract the grid phase, frequency and amplitude, owing to its simple structure and robustness. **Figure 51** shows the basic block diagram for the SRF PLL.

Assuming that the input voltage, *v*, is sinusoidal, it is expressed by

$$v = V\sin(\theta) = V\sin(\omega t + \emptyset) \tag{30}$$

where θ is the angular speed, ω is the angular frequency and φ is the phase. The output from the quadrature signal generator is:

$$v_{(\alpha\beta)} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = V\begin{bmatrix} \sin(\theta) \\ -\cos(\theta) \end{bmatrix} \tag{31}$$

Here, it should be mentioned that the quadrature signal generator is used for a single phase system, whereas for a three phase system abc/αβ transformation can be directly employed. By applying the αβ/dq transformation in (*32*), the output of the PD is expressed with

$$v_{(dq)} = \begin{bmatrix} v_d \\ v_q \end{bmatrix} = V \begin{bmatrix} \sin(\theta - \theta') \\ -\cos(\theta - \theta') \end{bmatrix} \quad (32)$$

From this equation, it is noted that the output of the PD is free of oscillations if the PLL is well tuned to the input frequency (ω≈ω').

In Figure 52, the output signals of the Quadrature Signal Generator (QSG) for the input vector v_n are represented in the stationary reference frame (defined by the *αβ* axes). The output signals of the *αβ/dq* transformation are represented by the projections of the voltage vector v_{in} on a rotating reference frame defined by the *dq* axes. The angular position of the *dq* axes, *θ'*, is given by the PLL. When the PLL is well tuned to the input frequency (*ω≈ω'*), the virtual input vector and the dq axes have the same angular speed. Consequently, the LF in **Figure 51** sets the angular position of the dq axes to make $v_d=0$ in the steady state.

The performance of the QSG in **Figure 51** is a critical factor for the determination of the accuracy of the PLL algorithm for a single-phase system. Some relevant techniques to generate a set of quadrature signals are reviewed in the following.

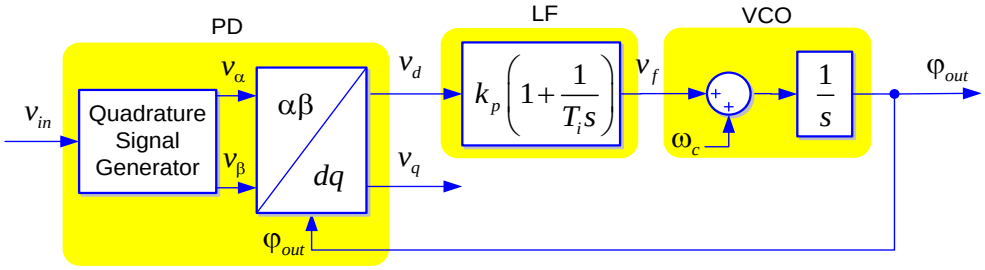


Figure 51: Synchronous reference frame PLL [37].

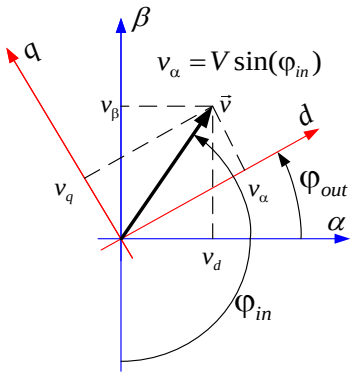


Figure 52: Vector representation of the QSG output signals [37].

PLL based on T/4 transport delay [37]

One common way to implement the PLL is to use a transport delay of one fourth of the fundamental period to realize the QSG function. This is shown in **Figure 53**. The T/4 delay block can be implemented with a first-in-first-out (FIFO) buffer, of which size is set to one-fifth of the number of samples for the fundamental frequency. This changes the frequency of the grid voltage and the output signal, v'_β is not perfectly orthogonal, which causes phase errors. In addition, if the grid voltage is distorted by low order harmonics (e.g. 3rd, 5th, 7th …), the low order harmonics generate oscillation in the estimated phase. As a disadvantage for this method, the T/4 delay block does not provide any filtering function. In summary, the features of the PLL are:

- Easy implementation using a first-in-first-out buffer
- Prone to changes in the grid frequency
- No filtering capability – affected by low order harmonics

PLL based on the inverse coordinate transform (αβ to dq) [37],[38]

The inverse coordinate transformation with low pass filter can be used to generate the orthogonal signal v'_β as shown in **Figure 54**. This simultaneously acts as a second order band pass filter for v_α to v_α' and a low pass filter for v_α to v'_β, whereby the frequency of these filters is given by the rotation speed of the synchronous reference frame. The advantage of this method is that v_α and v'_β are always in-quadrature and have the same amplitude in steady state, implying that it is robust against frequency variations of the grid voltage. In summary, the features of the PLL are:

- The orthogonal component is reconstructed by the direct/inverse coordinate transformation and the corresponding low pass filter.
- Not affected by grid frequency changes

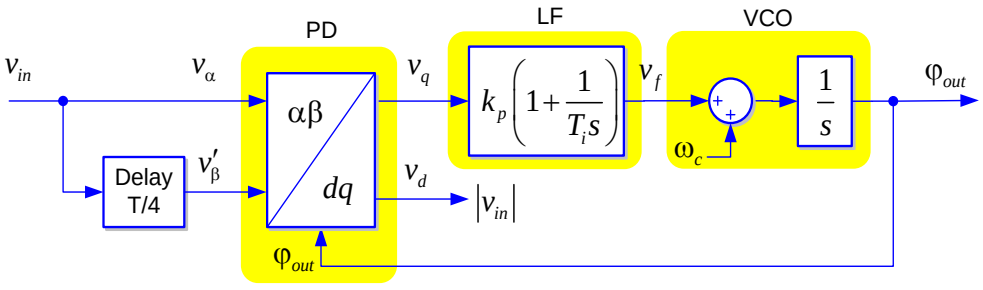


Figure 53: PLL based on T/4 transport delay.

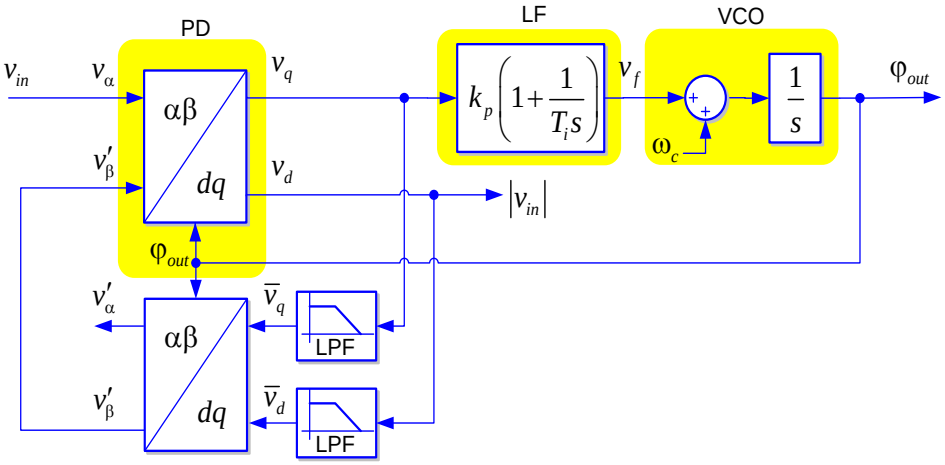


Figure 54: PLL based on the inverse coordinate transformation [37].

PLL based on the Second Order Generalized Integration (SOGI) [37] [38]

The SOGI consists of a second order adaptive filter, which is suitable for variable frequency application, because the bandwidth is determined by the gain k. In addition, the amplitude of *v'* and *qv'* matches that of the input signal *v*, when the frequency of the filter *ω'* matches the grid voltage frequency *ω*. The SOGI can be applied to implement the QSG block as shown in **Figure 55**, whereas this system has double feedback loop, for *θ'* and *ω'*. The relevant characteristics of the SOGI are:

- A second order filter is used to generate the orthogonal component without phase delay
- It is not affected by the grid frequency changes
- The dynamic performance can be tuned by the damping gain *k*
- The dynamic performance is limited by the inverse value of the resonant frequency *ω'*

The three PLLs are compared in Error! Reference source not found. with respect to their p erformance during a voltage sag, a phase angle jump, a frequency variation, harmonics, a DC offset and (white) noise on the input signal. The T/4 delay based PLL shows the fastest dynamic response under the voltage sag and phase angle jump, but in the case of frequency step the SOGI based PLL shows the shortest

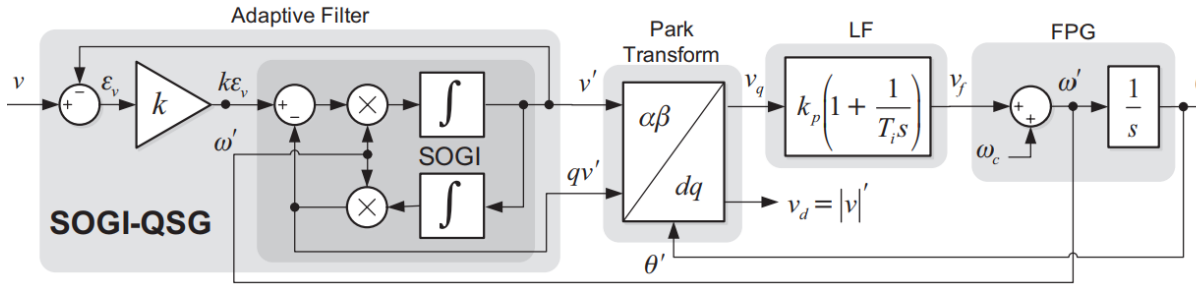


Figure 55: Diagram of the SOGI-based PLL (SOGI-PLL) [37].

Table 18: Performance comparison of single-phase PLL algorithms [39].

		T/4 delay PLL	Inverse coordinate transformation PLL	SOGI PLL
Voltage sag of -0.4	Settling time (5%)	22 ms	60 ms	55 ms
	Frequency overshoot	2.9 Hz	2.5 Hz	2.5 Hz
	Peak phase error	3.3°	6.7°	6.0°
Phase angle jump of 90°	Settling time (5%)	40 ms	81 ms	70 ms
	Frequency overshoot	17.0 Hz	18.9 Hz	22.0 Hz
	Peak phase error	16.2°	37°	25.0°
Frequency step of ±5 Hz	Settling time (5%)	70 ms	72 ms	53 ms
	Frequency overshoot	2.2 Hz	2.5 Hz	2.1 Hz
	Peak phase error	16.0°	17.0°	15.5°
Harmonics	Peak-peak frequency error	3.8 Hz	1.1 Hz	1.2 Hz
	Peak-peak phase error	0.8°	0.4°	0.4°
DC offset	Peak-peak frequency error	1.6 Hz	1.5 Hz	1.7 Hz
	Peak-peak phase error	1.7°	1.8°	1.9°
White noise (power = 0.01W)	Peak-peak frequency error	2.3 Hz	0.25 Hz	0.3 Hz
	Peak-peak phase error	0.4°	0.7°	0.8°

settling time. The inverse coordinate transformation based PLL and SOGI based PLLs feature similar performance for all cases, showing a better performance for the frequency step and harmonics than the T/4 delay based PLL.

b) Three-phase PLLs [40]

Instead of using single phase PLLs as described before, it is possible to utilize the symmetry of a three phase system for the detection of the grid angle. Five different three-phase PLLs are introduced and compared by means of their frequency, overshoot, the complexity, their performance during grid faults and the capability to detect phase jumps.

SRF-PLL (dqPLL)

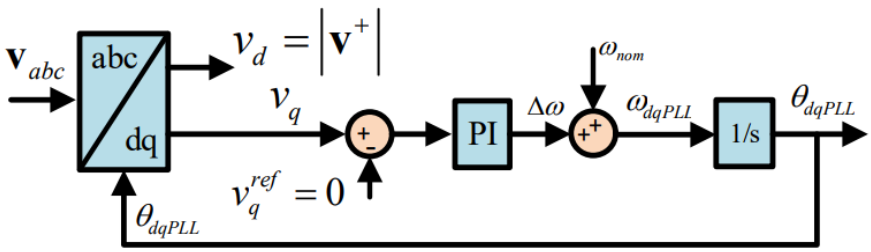


Figure 56: SRF-PLL for three-phase system [40].

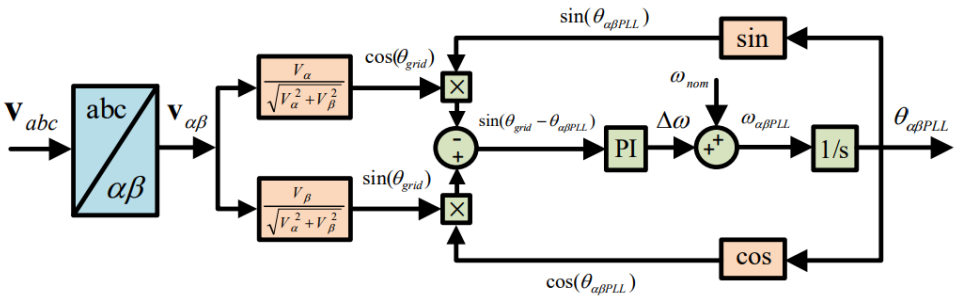


Figure 57: Structure of the αβPLL [40].

The SRF-PLL uses the abc to dq transformation to convert the signals from the abc frame to the dq frame as shown in **Figure 56**. To estimate the phase angle, the q component of the positive sequence voltage tracks a zero reference by PI control loop. As a result, the estimated phase angle becomes equal to the phase angle of the grid voltage and the d-component has the magnitude of the positive sequence voltage. This method can estimate the phase angle under balanced grid faults, but fails to track the phase angle under unbalanced grid voltage faults and harmonic distortions. In fact negative sequence components are caused by those faults, whereas the synchronous reference frame is rotating with the positive angular speed.

- The abc frame is directly converted into the dq frame without the QSG
- It operates accurately for balanced grid faults.
- It fails to track the angle when an unbalanced fault / harmonic distortion occurs.

αβPLL

The synchronization for the αβPLL is performed in the stationary reference frame as shown in **Figure 57**, where the trigonometric equations are used to calculate the error of phase angle. The phase angle error is fed to the PI control loop to track a zero reference. Similar to the SRF-PLL, the αβPLL fails to track the phase angle under unbalanced grid voltage due to negative sequence components. Even though the negative sequences can be filtered out with the lower bandwidth of the control loop, this results in a slower dynamic response. In summary, the αβPLL is characterised with the following points:

- It achieves synchronization in the αβ frame (directly converted from abc to αβ).
- The trigonometric calculation is used.
- A smaller frequency overshoot compared with the dqPLL.

- It estimates the grid angle accurately for balanced grid faults.
- It fails to track the angle when an unbalanced fault / harmonic distortion occurs.

Decoupled Double Synchronous Reference Frame PLL (dsrfPLL) (pre-filter based)

The methods introduced so far, SRF-PLL and αβPLL, fail to track the phase angle under unbalanced grid conditions, because of the negative sequence components. To overcome this, the SRF-PLL scheme is expanded by adding decoupling terms, which enable to separate the positive and negative sequence components. This method is called as dsrfPLL and the entire structure with the decoupling block is shown in **Figure 58 (a)** and **(b)**, respectively. The extracted positive sequence components are used to estimate the phase angle by the SRF-PLL. However, the grid voltage distortion is not considered. The important characteristics are:

- Pre-filtering block + dqPLL structure
- The positive and negative sequences of the grid voltage are decoupled by the pre-filtering.
- The extracted positive component is fed to the dqPLL to estimate accurate phase angle.
- It works accurately for unbalanced grid faults.
- The harmonic distortion is not considered.
- Slow dynamic response

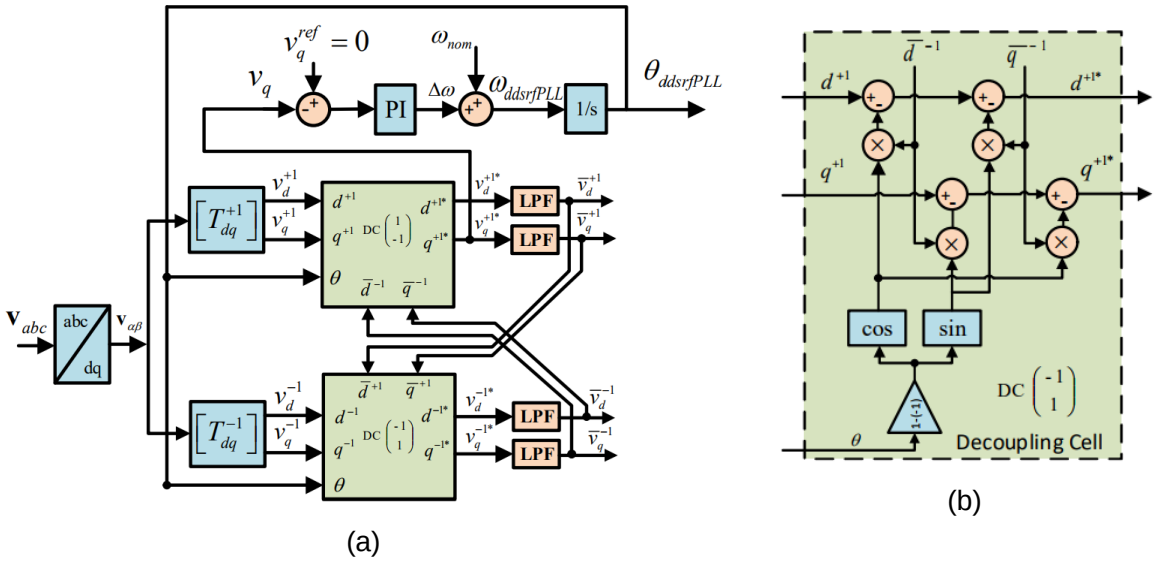


Figure 58: (a) Block diagram of the ddsrfPLL and (b) single decoupling cell [40].

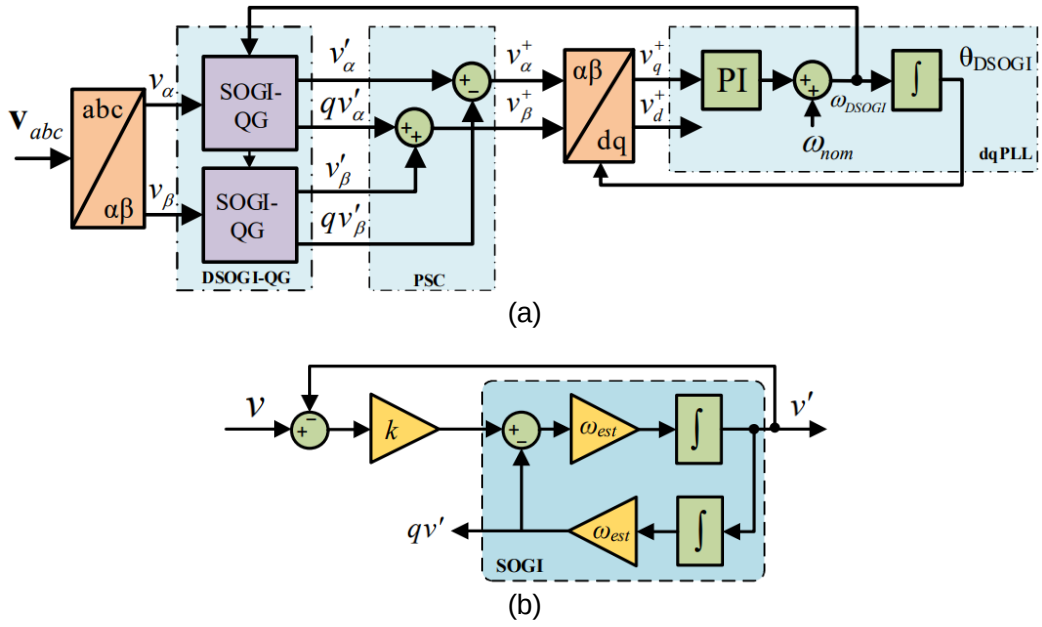


Figure 59: (a) Block diagram of the DSOGI-PLL and (b) SOGI block diagram [40].

Dual Second-Order Generalized Integrator (DSOGI) PLL (pre-filter based)

Similar to the dsrfPLL, the DSOGI-PLL aims at decoupling the positive and negative sequence components from the measured grid voltage. The positive sequence components are extracted in the αβ reference frame by two SOGI-QSGs as shown in **Figure 59**. The extracted positive sequence components in the αβ frame are transformed into the dq frame, which are fed to the SRF-PLL. In addition, the estimated frequency is fed back to the SOGI-QSGs to adapt the frequency of the SOGIs. However, the pre-filter based methods, dsrfPLL and DSOGI-PLL, feature a slow dynamic response due to the use of additional filters. In summary, the features of the DSOGI PLL are:

- DSOGI is designed in the αβ frame, which acts as an adaptive band pass filter.
- The positive component extracted from the DSOGI is fed to SRF-PLL
- It works accurately for unbalanced grid faults.
- Adaptive or Notch filter methods can replace the DSOGI block.
- Slow dynamic response

Frequency Phase Decoupling (FPD) dαβPLL (Loop filter modification based)

This method is based on the loop filter modification, of which objectives are the dynamic cancellation of negative sequence and/or undesired frequency components with a faster response and lower overshoot. In **Figure 60**, the loop filter modification is referred to as FPD, where the coefficient of integral term is adaptively adjusted to reduce the influence of frequency variation. Consequently, the frequency overshoot can be reduced, which results in a faster dynamic response. In summary:

- The loop filter is modified by the LFM method under the fault / disturbances of the grid voltage to improve the performance (especially, integral term is adjusted)
- Faster dynamic response / lower overshoot
- Mitigate the effect of undesired frequency variations under large abrupt disturbances in the voltage and/or phase angle.

The performance of the three phase PLL methods is summarized in **Table 19**. The conventional methods feature the simplest structure, whereas their performance is worst. The pre-filtering based methods shows the moderate performance for the overshoot and dynamic response under grid faults. The method based on the loop filter modification is complex to implement, but shows the best performance. Finally, the pre-filtering and loop filter modification based methods can accurately estimate the phase angle under unbalanced grid voltage and phase jumps, whereas the conventional methods are only capable detect the phase angle for a phase jump.

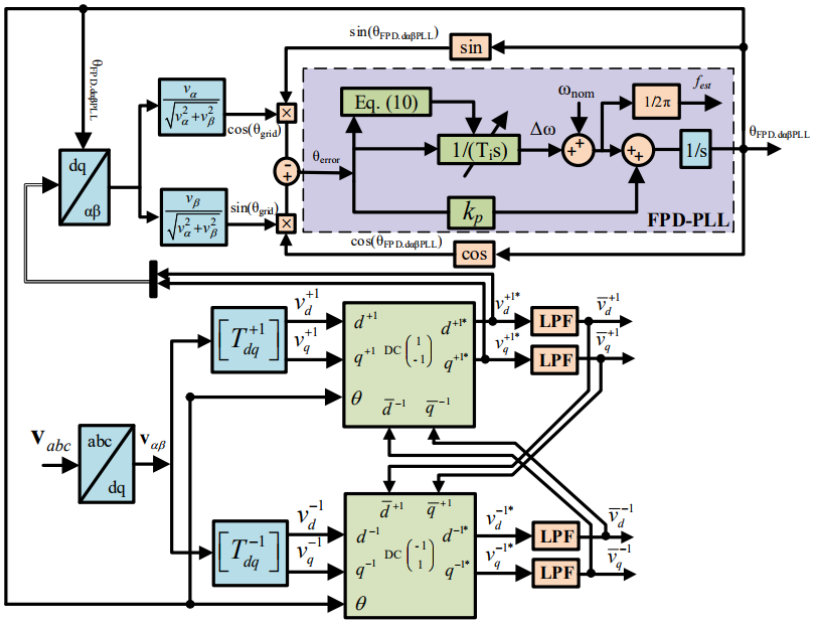


Figure 60: Block diagram of FPD based dαβPLL.

Table 19: Performance comparison of three-phase PLL algorithms [40].

	PLL algorithm	Frequenca/phase overshoot	Computational complexity	Dynamic response under grid faults
conventional	dq-PLL	High	Very low	Fast
	αβ-PLL	Low	Very low	Fast
Pre-filtering based	ddsrf-PLL	High	Low	Fast
	DSOGI-PLL	High	Low	Fast
Loop filter modification based	FPD dαβPLL	Very low	High	Faster

	PLL algorithm	Accurate Estimation under			
		Unbalanced	Harmonics	Phase jump	DC offset
conventional	dq-PLL	No	No	Yes	No
	αβ-PLL	No	No	Yes	No
Pre-filtering based	ddsrf-PLL	Yes	No	Yes	No
	DSOGI-PLL	Yes	No	Yes	No
Loop filter modification based	FPD dαβPLL	Yes	No	Yes	No

c) Alternatives to PLLs

As an alternative to the PLL, the virtual synchronous generator has been proposed. The virtual synchronous generator is a control scheme applied to the inverter of a distributed generating unit imitate the behaviour of a synchronous machine [41]. This concept is motivated by the traditional concept of the rotating synchronous generators. Virtual synchronous machines do not need a PLL for the synchronization in normal operation and force the power converter to behave like grid-forming devices improving the stability of the system in weak grid conditions.

3.1.4. Grid feeding control (power control)

The grid feeding mode (power control) is referred to the grid connected converter, which is controlled through the cascaded control loops as shown in **Figure 61**. The outer loop regulates the DC-link voltage and generates the grid current reference. The inner loop controls the grid current. The tuning of the inner loop is usually done such as the dynamic response of the system is maximized and the outer loop is designed in order to obtain a maximum phase margin. The tuning of the controller for the harmonic elimination is suggested to be tuned in such a way that the 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonics can be compensated. This usually refers to the harmonics, which are mostly affecting the grid power quality.

Voltage Oriented Control (VOC)

The VOC is based on the use of the dq frame, which is the synchronous reference frame rotating at the speed ω and it is usually aligned with the d axis of the grid voltage vector. Therefore, the space vector of the fundamental components is a DC-quantity in the dq frame. The control block diagram is shown in **Figure 62**, which consists of the DC-link voltage control (outer loop) and the grid current control (inner loop). The reference for the active power is generated as the sum of the power reference P^* and the output of the voltage controller. Then, the current references, i_d^* and

i_q^*, are generated. Generally, the active power is control by i_d, whereas the reactive power by i_q. Remarkably, this control scheme is suitable for the MV-side of the ST, whereas in the LV-side the four wires require to use an additional third controller as examined in section 1.1.2.

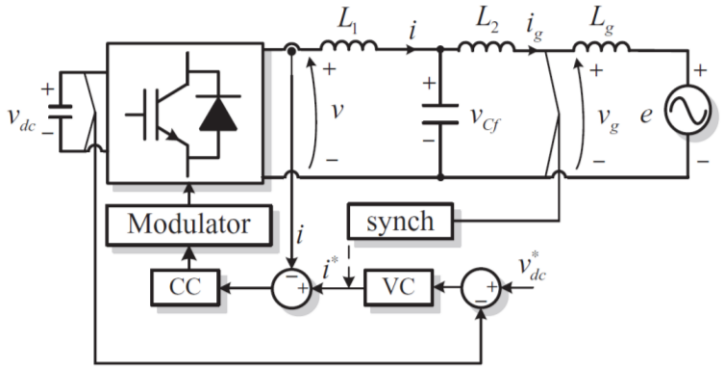


Figure 61: Cascaded control of the DC voltage (VC) through the AC current control (CC) for grid feeding mode operation [10].

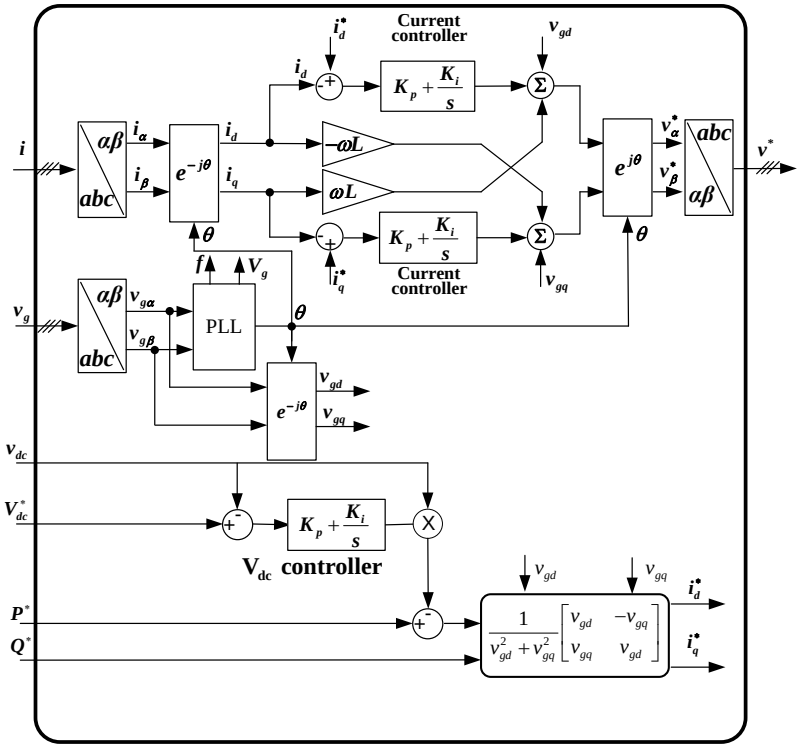


Figure 62: Control block diagram with PI current control for a three wire three phase system.

Direct Power Control (DPC)

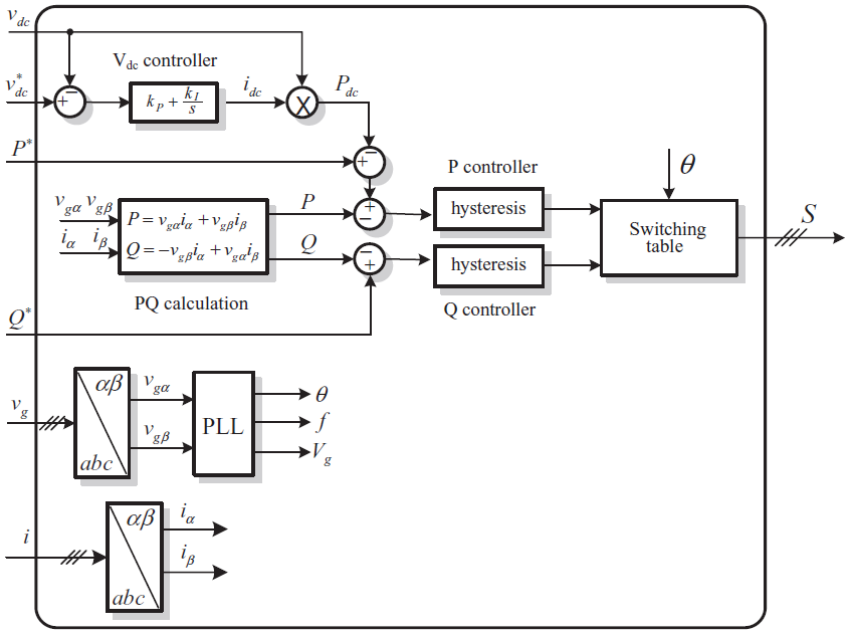


Figure 63: Direct Power Control (DPC) without PWM modulator [10].

In DPC concept, there are no internal current loops and no PWM modulator, because the converter's switching states are directly selected by a switching table based on the instantaneous errors between the commanded and estimated values of active and reactive power as shown in **Figure 63**. The main advantage is in its simple algorithm and a single control loop, whereas the main disadvantage is the need for a high sampling frequency to obtain good performance.

The modulator can be applied to the DPC method, but in this case the performance is equivalent with that of VOC method. In summary:

- There is no internal current loop (single control loop)

The active and reactive power loops behave like classical dq current loops in case the grid is stiff.

3.1.5. Grid forming control (voltage control)

In the grid forming (grid voltage control) mode, the converter operates as a voltage source to generate an AC voltage. Hence, the main challenges are related to the frequency and voltage control with a fluctuating of generated/consumed power. The control concept for the grid forming mode is shown in **Figure 64**. The AC voltage is directly controlled by the VC loop and its output is fed to the current control loop. In fact, the current control mainly contributes to prevent the over-currents. Therefore, a simple current limiter can replace the current control loop. In summary:

- Converter voltage is directly controlled
- A current controller is not required and a current limiter can add a voltage instead in order to prevent over-currents

3.1.6. Changing between grid feeding (power control) and grid forming (voltage control)

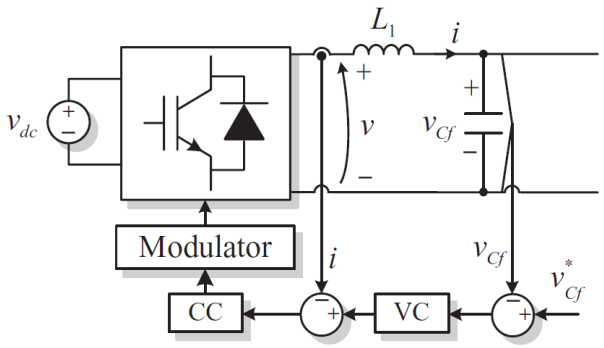


Figure 64: AC voltage (VC) with the AC current control (CC) for grid forming mode operation [10].

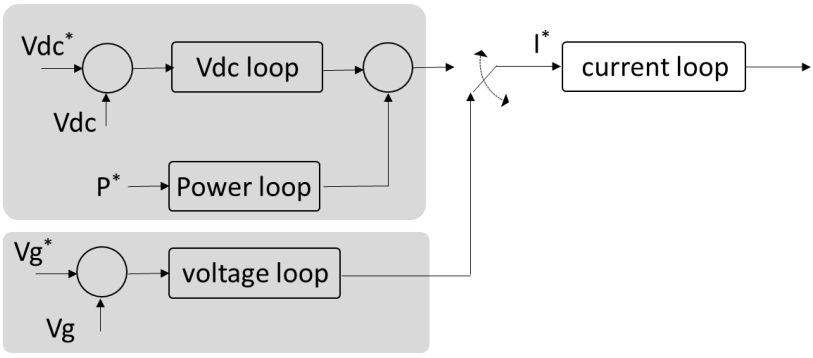


Figure 65: Basic configuration of control for two operation modes.

The transition between the power control and the voltage control is a challenging task, because the voltage command of the ST may oscillate because of the transition. The reason is that the output from both controllers may not be equal and voltage spikes or current oscillations may occur during the transition process. The procedure is visualized in **Figure 65**. However, for sensitive and mission critical loads, maintaining a

continuous and uninterrupted AC power is of importance and therefore, the transient conditions need to be controlled and an algorithm is required, which realizes a seamless transfer between the control modes. In the following, the transfer between the control objectives is described.

When the voltage is controlled and is supposed to be changed to power control (grid feeding control), the phase and amplitude of the load voltage of the converter must not change stepwise in order to prevent a perturbation of the grid voltage. Therefore, it is necessary that both the magnitude and phases of the converter's output voltage should be adjusted. The following steps should be performed [42, 43]:

- Detect that the grid is normally operating (no fault)
- Match the amplitude and phase of converter's reference output voltage
- Change the controller to grid-feeding control.

In a similar way, the transfer from grid-feeding control to grid forming control can be performed. First, the normal fault-free operation needs to be ensured and then the amplitude and the phase need to be matched for the output voltage of the two controllers. Once this is achieved, the control can be changed from grid-feeding control to voltage control.

Apart from the impact of changing the control mode on the single AC-stage, there is an impact on the control objective in the other stages. When the ST is operating in grid feeding control, the MV side converter regulates the (potentially distributed) MVDC-link voltage, the isolation stage controls the LVDC-link and the LV side converter regulates the LVAC voltage. In case the MV requires to operate in grid forming mode, it cannot control the MVDC-voltage anymore. Hence, the resulting challenge is the control of DC-link voltages, because both AC-converters operate in the grid forming mode. Furthermore, the energy needs to be provided to the ST, which is only possible if there is either an energy storage system connected to the ST or at least one connected converter enables to absorb the power from the connected grid.

3.1.7. LVDC grid voltage control

As examined in the report about ST topologies, DC-connectivity is a desirable feature of the ST. It can be realized in several ST architectures, which provide a DC-link or it can be realized with an additional ac/DC converter connected to the LVAC grids. In case the connection of the DC-grid is realized as a connection to the DC-link of the ST, another DC/DC converter is required to enable the control of the DC-grid. This is shown in **Figure 66** for an isolated DC/DC converter and a non-isolated DC/DC converter for the connection of the LV DC-grid to a DC-link. The grid voltage is set to 1.5 kV, which maximizes the capacity of the line within the specifications of “low voltage”.

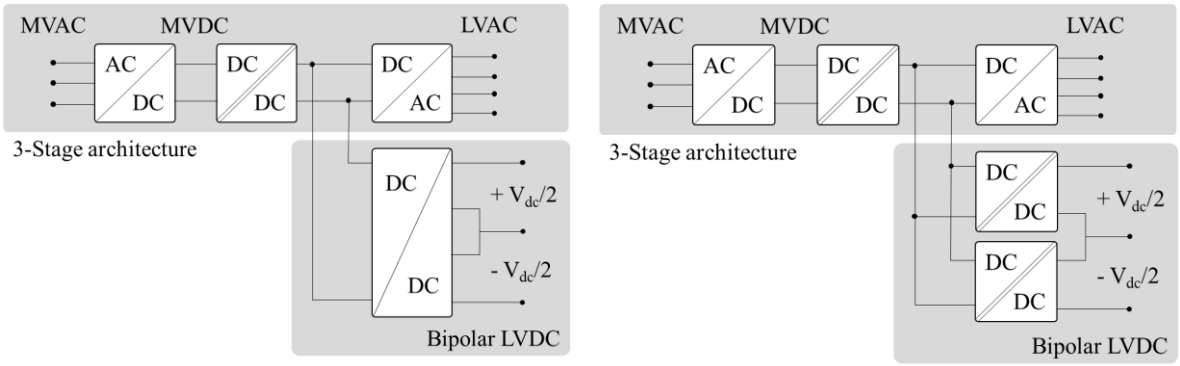


Figure 66: Three-stage architecture with a bipolar LVDC connectivity by (a) non-isolated DC/DC converter and (b) isolated DC/DC converter.

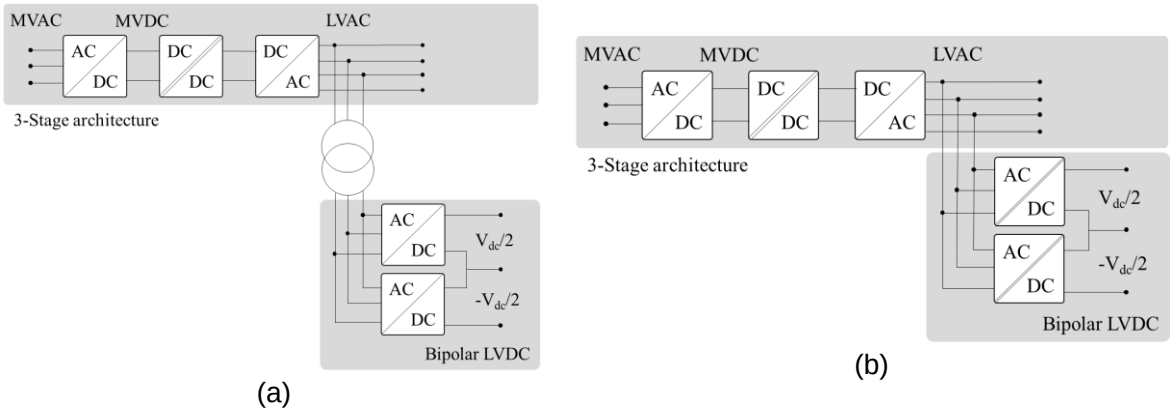


Figure 67: Three-stage architecture with a bipolar LVDC connectivity by (a) non-isolated AC/DC converter and (b) isolated AC/DC converter.

The connection of the DC-grid to the AC-grid is shown in **Figure 67**, whereas in **Figure 67 (a)**, it is shown for a DC-grid, which is isolated form the AC grid and in **Figure 67 (b)**, the DC-grid is not isolated from the AC-grid. As it can be seen in the figure, the power transfer from MVAC to LVDC is processed through four power conversion stages and one low frequency transformer. In comparison to the direct connection of the DC-grid to the DC-link, only three power conversion stages are processed. Therefore, a lower efficiency is expected in the power transfer from MVAC to LVDC if the DC-grid is fed from the LVAC grid. As another point to consider is the voltage level of the DC-grid, because high buck/ high boost ratios between AC/DC may reduce the efficiency of the topology or may require specially tailored solutions.

The block diagram of the DC-link controller is shown in **Figure 69**, in which it is assumed that there is a stiff LV DC-link voltage (i.e. it is regulated by the main circuit of the ST). Here, V^*_{LVDC} grid is the reference voltage of the LVDC grid and V_{LVDC} grid is the measured voltage. As the control loop, the PI controller can be employed.

The DC-grid voltage is expected to be controllable in a range of 0.9-1.1 p.u. Consequently, the required topology is dependent on the grid voltage and may be a buck converter, boost converter or a buck-boost. In case of the buck type, the LVDC-link should be bigger than the 1.1 p.u. of the LVDC grid, whereas it should be lower than 0.9 p.u. with the boost type. The buck-boost type can control the LVDC-link voltage in a wider range than the previous types.

If a DC-grid is considered to be connected to the DC-link of the ST, the capacitor of the DC-link needs to be sized appropriately. This means that it has to be sized not only for the power rating of the AC-grid, but for the overall power of the AC-grid and the DC-grid.

As examined before, the DC-grid can also be fed from the AC grid. The control block diagram for this case is shown in **Figure 68**. The control block diagram has a cascaded structure, consisting of the DC voltage (V_{LVDC} grid) and AC current (I_{LVAC}) control loops.

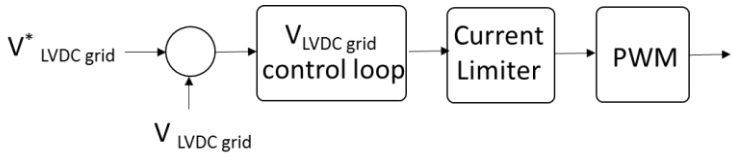


Figure 69: Control block diagram for a DC/DC converter regulating the DC-grid voltage.

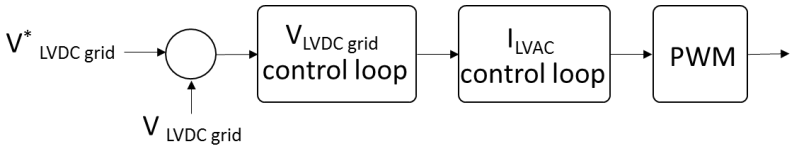


Figure 68: Control block diagram for AC/DC converter for the regulation of the DC-grid voltage.

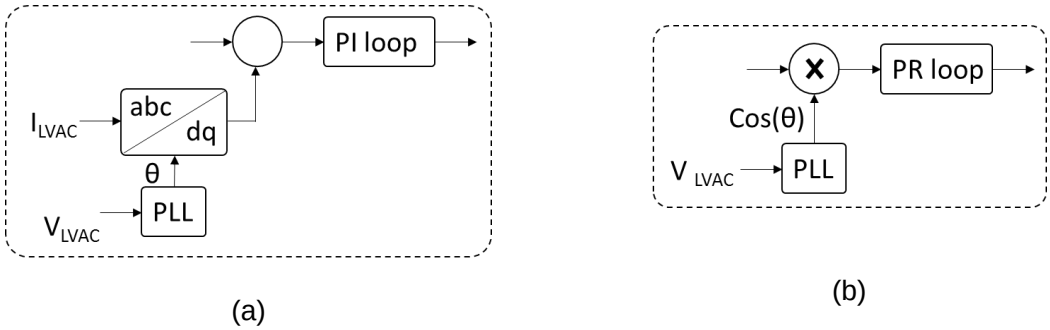


Figure 70: Possible AC current control loops in the rotating reference frame and the stationary reference frame: (a) PI loop and (b) PR loop.

The AC current control loop can be realized either with a PI controller or a PR controller as shown in **Figure 70 (a)** and **(b)**, respectively. For the PI-controller, the LVAC current is controlled in the rotating (dq) reference frame and the PLL algorithm is required to estimate the phase angle of the LVAC voltage. Similarly, the phase angle needs to be estimated for the PR loop, but the current is directly controlled in the synchronous (abc) reference frame.

The AC/DC converter is a boost type if the voltage ratio of transformer is 1:1 and the DC-grid obtains a voltage of V_{dc} =1.5 kV. To guarantee the control capability from 0.9-1.1 p.u. of the LVDC grid, the LVDC-link voltage should be lower than 0.9 p.u. of the LVDC grid.

As it can been seen, the control strategy for the DC/DC converter is much simpler than that for AC/DC converter, because the PLL and the transformation are not needed. Instead, the voltage control can be performed with a single control loop (in contrast to a cascaded controller), which shall provide a possibility to achieve a high bandwidth of the controller (i.e. fast control performance) with the same operating condition.

3.1.8. Summary of challenges in the controller design

The control of the ST has been introduced and the control objectives are explained for the example of a three-stage ST architecture. The control modes of grid forming (voltage control) and grid feeding (power control) have been addressed and the transition between the control modes has been described. As a challenge for the control of the ST, the exchange from grid forming in the MV-side and grid feeding in the MV side has been highlighted.

Another important point is the choice of the reference frames for the controllers, which are also dependent on the employed ST architecture.

The control of the DC-grid has been described for the connection of the grid to the DC-link of a ST or to the LVAC grid. The control in the stationary reference frame and the control in the rotating reference frame have been described for the DC-grid, which is fed from the LVAC grid and it has been concluded that the control of the DC-grid fed by a DC-link is preferred. Furthermore, it has been described that four power conversion stages and one low frequency transformer are required, if the DC-link is supposed to be isolated from the MV grid, whereas the direct connection to the LVDC-link requires only three power conversion stages.

3.2. Controller implementation

The controller can be implemented with various different hardware and different controller designs. The digital controllers are performing the control, generate the PWM, perform the Analog Digital Conversion (ADC) and realize the communication. Particularly the complexity of a modular power converter with multiple converter stages results in the challenge of data acquisition speed, synchronization of building blocks and reliability of the high number of components. For this purpose, different hardware will be discussed in this section. Digital control is state of the art and it is commonly implemented in Digital Signal Processors (DSP)s and Field Programmable Gate Array (FPGA). In the following, these two devices are described as representative examples for the controller implementation. The implementation of the controllers in DSPs and FPGAs is addressed and different communication interfaces are presented. Finally, the operation with a Master and Slaves is discussed.

Features of DSP and FPGA

The use of DSPs makes the implementation of a complex algorithm easy and flexible, because the software is handled in series sequence. In addition, by means of appropriate built-in peripheral modules, the hardware functionalities such as PWM and ADC are realized. Especially, the floating-point DSP is an attractive solution for applications with data sets requiring real arithmetic, because it provides the mathematical flexibility, the accuracy, the smaller execution time and the reduced development time. However, the main drawback of DSPs (both fixed- and floating-point) is that the size of the integrated periphery is limited.

In contrast to the DSP, the software of the FPGA operates in parallel. This means that multiple tasks can be performed simultaneously, which provides higher performance in repetitive computations. However, it is much more difficult to implement intensive arithmetic operations and trigonometric calculations in the FPGA. The reliability of the FPGA was predicted to be ten times worse than the DSP [44].

The combination of DSP and FPGA has been proposed in order to exploit different advantages of each controller [46, 47]. However, one of the issues is the communication between them, which directly determines the performance of the whole control system. In the following, approaches will be described, which target the combination of the introduced control hardware.

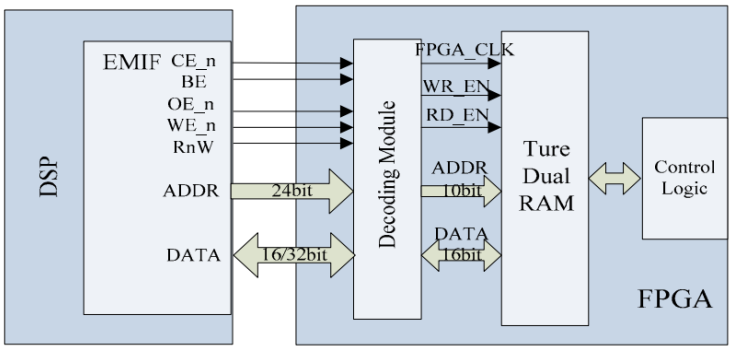


Figure 71: EMIF interconnect between DSP and FPGA [45].

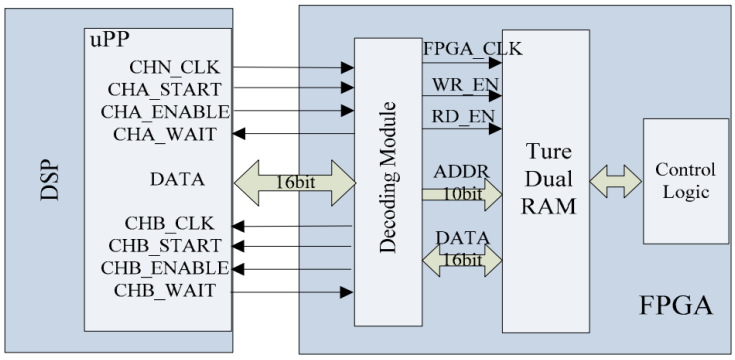


Figure 72: uPP interconnect between DSP and FPGA [45].

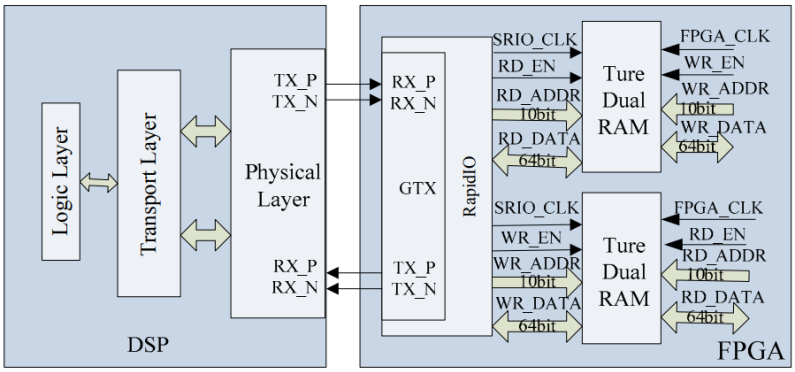


Figure 73: RapidIO interconnect between DSP and FPGA [[45].

Communication interfaces for DSP+FPGA [45]

For the combination of DSPs and FPGAs, there are several possibilities. One of them is an External Memory Interface (EMIF): The EMIF is a typical high-speed parallel interface, which has strong peripheral connectivity capabilities and fast data transfer capability. The EMIF interconnection of the DSP and FPGA is shown in **Figure 71**.

Another possible communication interface is the Universal Parallel Port (uPP): The uPP is a multi-channel, high-speed parallel interface with dedicated data lines (transmit or receive) and minimal control signals. This can operate in receive mode, transmit mode, or duplex mode. The connection of uPP between DSP and FPGA is shown in **Figure 72** and in this configuration, the frequency of the DSP limits the maximum data transfer rate.

The third possible interface is RapidIO. The RapidIO shows a high performance by high data bandwidth, low latency and scalability. In addition, the automatic data validation and error detection function guarantees the high reliability and the small number of I/O facilitates the expansion to achieve peer-to-peer data communication. The DSP and FPGA connection via the RapidIO is shown in **Figure 73**.

The PCI Express (PCIe) is a full duplex and high-speed differential serial interconnect bus, which uses the master-slave structure. The interconnection pattern for the master-slave structure can be the point-to-point or the tree structure. The PCIe provides the ideal support for hierarchical structure and it has flexible bandwidth and scalability. The manner of PCIe interconnect is shown in **Figure 74**.

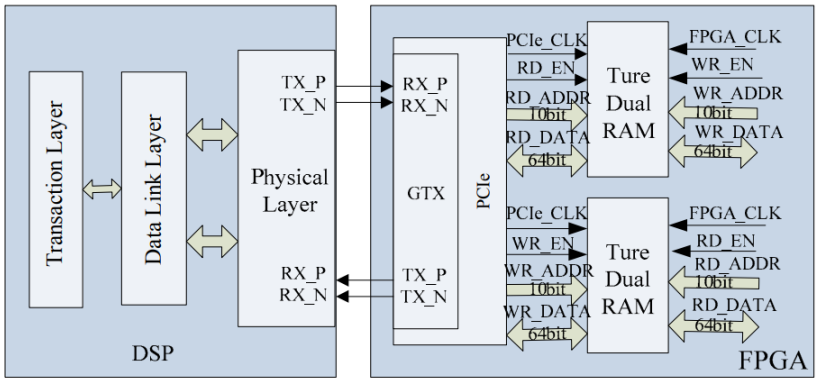


Figure 74: PCIe interconnect between DSP and FPGA [45].

Considering the 125 Mhz clock and 128B data transmission, the four communication interfaces are compared in **Table 20**. Thereby, the “theoretical link rate” is the rate of no overhead and the “theoretical communication rate” is the interconnection overhead between DSP and FPGA.

The EMIF and uPP are parallel communication interfaces and have not specific bus protocol, which enables a simple realization. In comparison to these two interfaces, the uPP is faster and requires less I/O count. The RapidIO and the PCIe have many similarities; especially the interconnection communication rate is very similar. Their transmission rates are higher than the previous two methods, so that they are suitable for applications on chip-level and backplane-level interconnection, especially for large amounts of data transmission.

Finally, it is worth noting that if a single communication interface interconnection does not meet the demands, a high-speed serial and parallel interface combining communication scheme can be considered.

Table 20: Comparison of interface communication [45].

Interface scheme	EMIF (16/32)	uPP	RapidIO	PCIe
Communication method	Half duplex	Full duplex	Full duplex	Full duplex
System mode	Master/slave	Peer to peer	Peer to peer	Master/slave
Theoretical link rate (Gbps)	0.5/1.0	1.0	2.5	2.5
Theoretical communication rate (MBps)	35.71/71.43	125	205.13	216.22
Protocol overhead	0	0	28	20
I/O	>=46/62	>=24	4	4
Data type	Batch/Burst	Batch/Burst	Batch	Batch

3.2.1. Centralized controller

Apart from the controller implementation, it is possible to design a centralized controller or to distribute the control of the system. The centralized controller collects all information and performs the required calculations before sending back the new control commands. The decentralized controller instead enables to perform certain computations or even control loops in local control loops. In the following, the master-slave control strategy, the peer-to peer controller and finally the multi-agent controllers are introduced.

Master-slave control strategy [48]

In master-slave control, certain operations can be performed by the slaves, whereas others are operated by the master controllers. As an example for the control of a ST, the slaves are operating in grid feeding control and send their measures to the master controller. The master controller performs the grid optimization and controls the voltage and the frequency. As a requirement for the active power balancing, the master controller needs to have sufficient current capacity to generate the grid voltage and/or the communication needs to be fast enough to enable the support of the slaves with active and reactive power. The centralized controller can be implemented in the ST or decentralized. This is referring to the scenario of a ST fed microgrid and it is demonstrated in **Figure 75**. In summary, the features of the master-slave control are:

- The master source capacity should be large enough in order to ensure a stable voltage and frequency.
- A communication system is required to arrange the load sharing among the micro terminals, which can be multiple STs connected to a grid in this case.
- The dependence of the control scheme on the master source and the communication system result in a high dependence and may influence the reliability of the system.

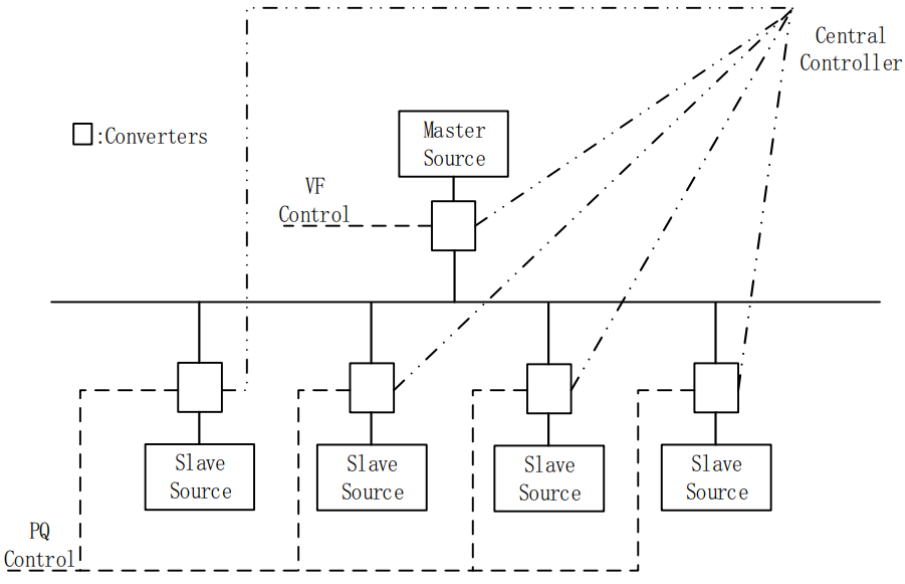


Figure 75: Architecture of master-slave control as an example, where the slaves control the apparent power control and the master the voltage and the frequency [43].

3.2.2. Decentralized controller

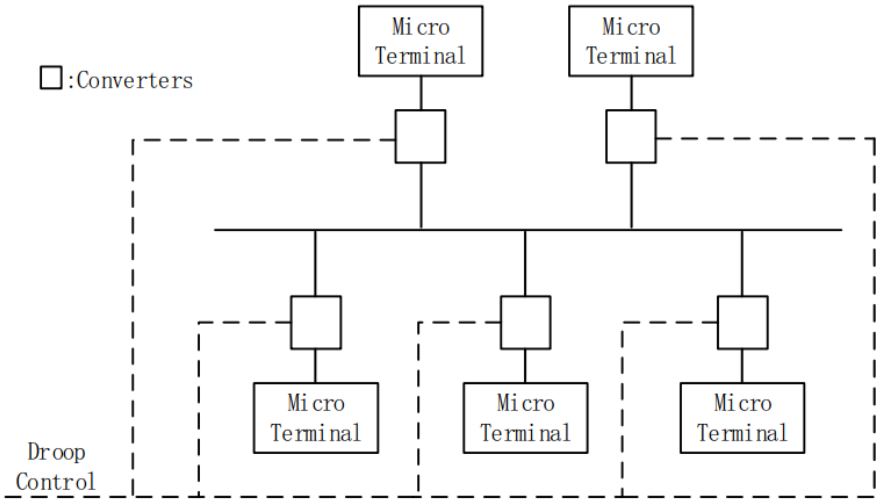


Figure 76: Architecture of peer-to-peer control [43].

A decentralized controller only relies on local information for the control of a system, which is referred to as peer-to-peer control and shown in **Figure 76**. It does not use communication and the load shedding etc. needs to be realized in a different manner. One of the possible ways to realize this is a droop controller. In summary, the peer-to-peer control is characterized by [48]:

- Converter control is performed with local information. Therefore, no communication system is required
- All micro terminals support the bus voltage and the frequency of the system. This is done according to the predefined droop characteristics. (It does not rely on a specific micro source).
- There needs to be a frequency and voltage drop controller with implemented droop characteristics.

Multi-agent control [48]

Another opportunity to realize the control is a multi agent control system as shown in **Figure 77**. Autonomous agents use local information and neighbour-to-neighbour communication to achieve cooperative objectives. Therefore, it requires communication systems with neighbouring micro terminals. In this way, communication can be processed through different ways to the other agents and commonly used methods from communication theory may be adopted. In summary:

- A communication system is required, which only communicates locally with its neighbourhood (differently with the centralized control).
- In contrast to the centralized controller, there is no master and loss of an agent may not be impacting the system

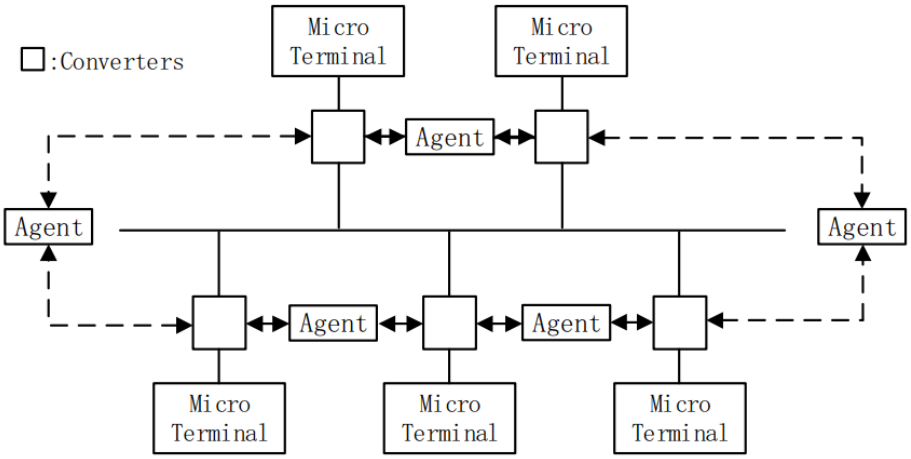


Figure 77: Architecture of a multi-agent control system [43].

3.2.3. Implementation of centralized and de-centralized control capability

The control of the ST requires covering periods in the range of multiple kHz to several minutes. This requires using different control frequencies and the consideration of the response time for each of the control loops as well as consideration of the required communication speed. The implementation of such control system in a centralized way leads to the challenges with respect to the loss of communication (either completely or loss of communication or loss of several data packages).

Therefore, the implementation of the control system should be done with controllers implemented on a local level (substation level), whereas other functionalities are implemented in Smart control units, which are exchanging information with other meters and substations in the grid. As an example, the voltage/current control of the ST needs to be implemented locally, because the sampling frequency of the data acquisition needs to be in the rage of several kHz. Other control functionalities, like the voltage/power reference generation can be set by the Smart control unit, which collects data from additional sources (like smart meters) and exchanges them with other Smart Control Units. This concept is visualized in **Figure 78**, where the potential communication flow of the ST control is visualized [49]. The variables to be sensed in the ST are shown in **Table 21**.

Within the substation level control, the ST control can also be implemented in a centralized manner or in a distributed way as it was explained in the previous subsection. However, this is highly dependent on the adopted ST architecture and it will affect the reliability, the required communication speed and the synchronization requirements.

Acquisition and storage of data with a high sampling rate results in a high amount of data, which may not be needed for post-processing the data. However, for failure analysis it is recommended to log the data for a certain period, so that the sensed parameters are stored once a grid fault occurs or a device is failing. This enables to perform root cause analysis and potentially supports in preventing similar failures in the future.

Table 21: Sampling frequencies for the variables in the system.

Figure 78: Minimum data acquisition requirements [49].

	Sampling frequency	Comments
LV AC-grid currents/voltages	f_s, ~5-20 kHz	Control frequency, dependent on the harmonic order to be compensated
MV AC-grid currents/voltages	f_s, ~5-20 kHz	Control frequency, dependent on the harmonic order to be compensated
MV AC-grid power	> 1 min (time stamped)	Smart meters distributed in the grid
LV AC-grid power	> 1 min (time stamped)	Smart meters distributed in the grid
Voltage at NOPs (magnitude, phase, frequency)	> 1 s (time stamped)	Meters at NOP, much slower sampling possible
MV harmonic distortion of the voltages/currents	> 1 min (time stamped)	Harmonic order, magnitude, phase sensed by smart meters
MV harmonic distortion of the voltages/currents	> 1 min (time stamped)	Harmonic order, magnitude, phase sensed by smart meters

3.2.4. Transition between LFT fed grid and ST fed grid

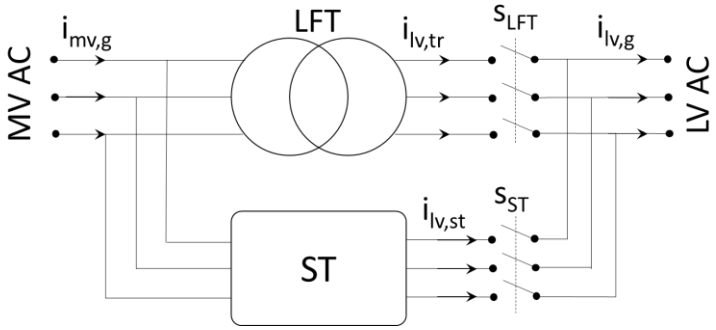


Figure 79: Change of the power transfer between ST and LFT during connection of the ST and continuous operation of the LV grid.

In this subsection, the procedure to switch between the operation of a LFT and the ST is explained. The system of the parallel connected LFT and the ST is shown in **Figure 79**. This is required for the start-up of the ST, because the LVAC-grid is expected to continue to operate, even while the ST is installed. Therefore, $i_{lv,tr}$ and $i_{lv,st}$ need to be measured and the ST is controlling $i_{lv,st}$. Initially, all power is assumed to be processed through the LFT (S_{LFT} is close and S_{ST} is open). As first step, the ST is started (charging of DC-links) and connected to one side of the grid (MV-side in this case). In the LV side, the switch S_{ST} is closed and the current control ($i_{lv,st}$) of the ST is activated with zero current reference. For transferring the power transfer from the LFT to the ST, the current reference of the ST is increased ($i_{lv,st}$) until the LFT current ($i_{lv,tr}$) becomes zero. Finally, the switch S_{LFT} is opened.

Table 22: Communication standards comparison for smart grid applications [50].

Technology	Standard	Data rate	Distance	Network
PLC	Ultra-narrowband	100 b/s	150 km or more	Core
	Narrowband	10-500 kb/s	10 km or more	Wide area
	Broadband	1-200 Mb/s	1 km	Private
DSL	High-bit-rate	1.5-24 Mb/s down, 0.5-3.5 Mb/s up	1.6-18 km	Private/wide
	Asymmetric	256 kb/s-2.3 Mb/s	Up to 5.5 km	Private
	Symmetric	256 kb/s-2.3 Mb/s	Up to 3 km	Private
	Very-high-bit-rate	55-100 Mb/s down, 3-100 Mb/s up	300 m	Private
Wireless mesh	IEEE 802.11	6-54 Mb/s	0.1-5 km	Private/wide
	IEEE 802.15	11 Mb/s – 5.3 Gb/s	20-100 m	Private
Cellular	2.5 G	40-500 kb/s down, 9.6-42.8 kb/s up	Up to 200 km	Wide/core
	3 G	200 kb/s-2 Mb/s	10-72 km	Wide
	3.5 G	14-337 mb/s down, 5.76-34 Mb/s up	5-20 km	Private/wide
	4 G	100 Mb/s-1 Gb/s down, 50-500 Mb/s up	3-30 km	Private/wide

If the power transfer shall be transferred from the ST to the LFT, the same procedure needs to be followed in the inverse way. Initially, all power is processed through the ST (S_{LFT} is open and S_{ST} is close) and the switch S_{LFT} is closed. In the next step, the current transferred by the ST is controlled to zero and finally, the switch S_{ST} is opened and the LFT transfers the whole power.

3.3. Possible communication interfaces

The communication of a ST-fed grid can be categorized by the different senders and receivers. This requires different communication speeds and therefore different communication protocols. The first kind of communication is data transmission between smart meters and distributed energy resources, power-line communication (PLC). Therefore, a local area wireless network, such as the family of IEEE 802 network can be applied. The second kind of flow is between the ST and local electric appliances. The third flow is between the ST and the data centre or between two different STs (if multiple STs are applied in the grid). The latter two types of information flow require higher data transmission rates and wider coverage areas, which can be accomplished by a wide area network, including a cellular network and digital subscriber line (DSL). A selection of possible communication technologies in ST-fed grids is shown in **Table 22**.

4. Reliability considerations

This subsection provides a review on reliability and discusses challenges for the reliability of the ST. Components with high expected probability for failures are identified and their failure mechanisms are examined. Innovative methods to improve the reliability of these components are introduced. Operation and Maintenance concepts are discussed and finally, requirements for the reliability of the ST design are concluded.

4.1. Definition of reliability and introduction of availability

The term reliability has been subject to multiple definitions, but still no commonly accepted definition has been found. For clarification of the definition, in this work, reliability is defined as ability of a component to perform a required function under given conditions for a given time interval. Therefore, the functionality is important to be defined (e.g. full capability or reduced capability) and the time period for which this needs to be provided. In the following, the reliability is addressed and basic concepts for the reliability investigation are discussed.

The reliability of a system is commonly represented by means of the failure rate over time. This can be separated into [51]:

- Early failures
- Random failures
- Wear-out based failures (physics of failure)

The early failures are commonly related to damage during transport, wrong installation etc. and can hardly be addressed without the knowledge of the supply chain. Their probability is usually high at the commissioning and reduces over time. Random failures can be modelled with a constant failure rate over time and represent failures, which cannot be traced back or which have a random probability distribution, e.g. cosmic ray induced failures in power semiconductors. The constant failure rate λ is represented in (33):

$$\lambda = \frac{n_1 + n_2 + \cdots + n_i}{N_1 T_1 + N_2 T_2 + \cdots + N_i T_i} \cdot 100\% \tag{33}$$

Here, n_i is the number of failures by the i-th population, N_i is the number of transformers of the i-th population and T_i is the reference period of the i-th population. The wear-out based failures are occurring after a specific time in operation and increase over time, whereas they do not occur at the beginning of the lifetime.

Several publications/companies refer to reliability and apply the constant failure rate for the qualification of their products [52, 53]. However, this does not provide any comprehensive information about the required lifetime of a component, because the failure rate is obtained from reliability tests performed on a large number of components, which implies it cannot be directly interpreted as the lifetime of a single component. In other words, it assumes testing *n* samples for the reference period T_i is leading to similar results as testing a single device for $T_i \cdot n$ minutes. This has been found to be insufficient in many cases and wear-out based failure mechanisms were studied to understand the aging and failure mechanisms [54]. In this way, the analysis gets much more complicated, because the mechanisms can be considered for all devices and mechanisms in a system.

A method to take the different failures into account is the Failure Distribution Function (FDP), which is defined as the time at which a certain percentage of the components are failed. This is shown in **Figure 80** and can be calculated from the unreliability curve given by (34):

$$F(t) = \int_0^t f(t)\,dt = 1 - exp\left[-\left(\frac{t-\gamma}{\eta}\right)^{\beta}\right] \quad (34)$$

Here, α, β and γ are the Weibull parameters [55] and *f(t)* is the failure distribution function, which gives a cumulative probability for a failure.

Based on the unreliability curve, the B_x lifetime can be determined, which is referring to the time at which *x %* of the devices have failed. For a single device, it corresponds to a failure probability of *x* percent. The plotted unreliability curve in **Figure 80**, shows a B_1 lifetime of 20,6 years and a B_{10} lifetime of 21,2 years.

Apart from the definition of reliability, the availability is of high important to identify the undesired off- time and repair time for the consideration of repairable systems. The definition of availability A is the time in operation $T_{operation}$ divided by the sum of the time in operation and the off-time $T_{interruption}$ as expressed in (35).

$$A = \frac{T_{operation}}{T_{operation} + T_{interruption}} \quad (35)$$

The availability is independent from technical solutions and faulty components. It only refers to the time in which the system is performing its functionality. A requirement for availability is of importance and an assessment by this means may encourage the manufacturers to provide very reliable solutions.

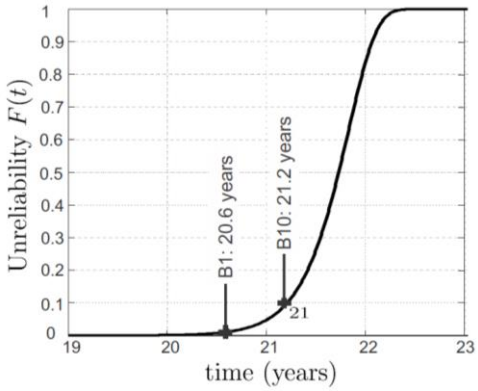


Figure 80: Unreliability curve with Bx lifetime.

4.2. Reliability of the ST

The ST as a power electronics converter consists of a high number of components, such as power semiconductors, capacitors, inductors and driver circuits, which can possibly fail. The failure of a single device commonly results in a down time of the whole system or the whole building block. Therefore, it is of interest to identify the most sensitive components and to prevent their failure or to limit the impact of any failure on the operation of the system. In the following, first the impact of an outage of the ST on the network is evaluated based on the five LV Engine schemes and then the failure mechanisms and the related design impact to address the failures is described.

4.2.1. System level impact of the ST failure

Considering the five LV Engine schemes, a failure of the ST may lead to the disconnection of a grid feeder or may have limited impact on the grid operation. Therefore, the impact of a failure in the ST on the operation of the grid is evaluated and summarized in **Table 23**. For scheme 1 and

scheme 2 with a single ST, the power supply of the grid is interrupted if the ST is not operating and the NOP is open. If the NOP is closed, the LFT has to supply the whole power to the grid and it may be overloaded or the voltage profile in the grid may violate the norms. In case of scheme 3, the power control is required when one of ST fails, which aims at avoiding the overloading of the healthy STs. Similar to scheme 2, the voltage profile may be violated in this case. For the scheme 4 and 5, a failure of the ST interrupts the power supply to the grid.

In order to avoid load shedding or even the disconnection of a grid feeder, the redundancy of the ST can be utilized. As highlighted before, redundancy can be employed on different level, such as: system level, topology level and building block level. This issue is addressed in the section 0 and can be used to evaluate the costs for the desired redundancy.

Table 23: Impact of ST outage in different LV Engine schemes.

LV Engine scheme	Failed ST	NOP status	Impact on the distributed grid	Control requirement
Scheme 1	ST (substation A)	Open	• Interrupted power supply to loads connected to substation A	-
		Close	• Possibly overloaded LFT in substation B	-
Scheme 2	ST (substation A)	NOP1: Open NOP2: Open	• Interrupted power supply to loads connected to substation A	-
		NOP1: Open NOP2: Close	• Possibly overloaded LFT in substation C	-
		NOP1: Close NOP2: Open	• Possibly overloaded LFT in substation B	-
		NOP1: Close NOP2: Close	• Possibly overloaded LFT in substation A and B	-
Scheme 3	ST (substation A)	NOP1: Open NOP2: Open	• Interrupted power supply to loads connected to substation A	-
		NOP1: Open NOP2: Close	• Possibly overloaded LFT in substation C	-
		NOP1: Close NOP2: Open	• Limited power to loads connected to substation A by ST in substation B	Power control to avoid over loading of ST in substation B
		NOP1: Close NOP2: Close	• Limited power to loads connected to substation A by ST in substation B	Power control to avoid over loading of ST in substation B
	ST (substation B)	NOP1: Open NOP2: Open	• Interrupted power supply to loads connected to substation B	-
		NOP1: Open NOP2: Close	• Interrupted power supply to loads connected to substation B	-
		NOP1: Close NOP2: Open	• Limited power to loads connected to substation B by ST in substation A	Power control to avoid over loading of ST in substation A
		NOP1: Close NOP2: Close	• Limited power to loads connected to substation B by ST in substation A	Power control to avoid over

				loading of ST in substation A
	ST (substation A and B)	NOP1: Open NOP2: Open	• Interrupted power supply to loads connected to substation A and B	-
		NOP1: Open NOP2: Close	• Limited power supply to loads connected to substation A by LFT • Possibly overloaded LFT in substation C • Interrupted power supply to loads connected to substation B	-
		NOP1: Close NOP2: Open	• Interrupted power supply to loads connected to substation A and B	-
		NOP1: Close NOP2: Close	• Possibly overloaded LFT in substation C	-
Scheme 4	ST (substation A)	-	• Interrupted power supply to DC grid	-
Scheme 5	ST (substation A)	-	• Interrupted power supply to DC grid and LV AC grid	-

4.2.2. Reliability of components in power converters

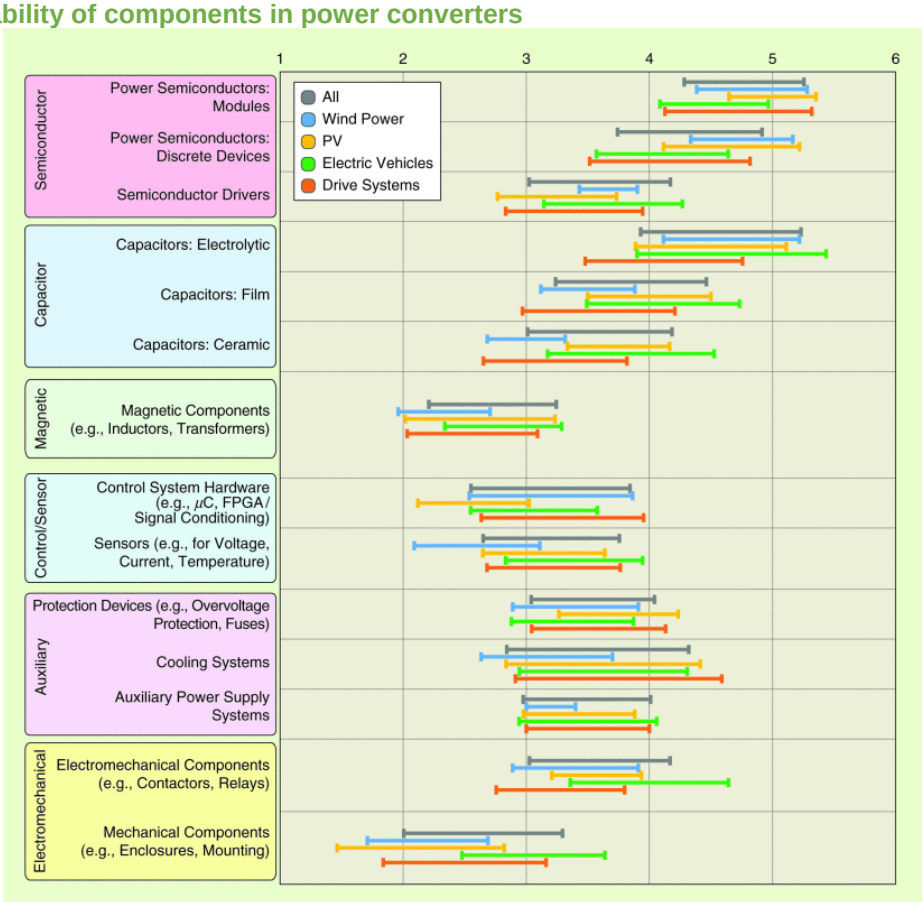


Figure 81: The critical components of power electronics systems by application in the opinion of industry experts [56].

In a recent industry survey, the expected most frequent failing components were requested from companies within the ECPE (European Centre for Power Electronics) and the results are shown in **Figure 81** [56]**.** As it can be seen, the power semiconductors and the capacitors are considered to be most frequently failing components. Other relevant components are the auxiliary components, meaning the protection devices, cooling systems and auxiliary power supplies. The components in the power electronics systems are exposed to different level of stressors depending on application and operating condition. This means that the influence of the application-relevant stress needs to be analysed. The survey about the application-relevant stress is shown in Fig 2, considering wind power, PV, electric vehicles and drive systems [56].

An analysis of the stressors for the most sensitive devices was performed in [57] is shown in **Table 24**. As it can be seen, the reliability of active power components and solder joint is highly affected by the temperature swing and average temperature, whereas the humidity influences on the reliability of ICs and PCB.

Table 24: The focus point matrix in reliability of power electronic components [57].

Load			Focus Points									
Climate + Design -> Stressor			Active Power Components			Passive Power Components		Control Circuitry, IC, PCB, Connectors				
Ambient	Product design	Stressors	Die	LASJ	Wire bond	Cap	Inductors	Solder Joint	MLCC	IC	PCB	Connectors
Relative humidity	Thermal system	Temperature swing	3	3	3	-	-	3	-	-	-	-
Temperature	Operation point	Average temperature	2	2	3	2	-	2	2	1	1	1
-	On/Off power	dT/dt	1	1	1	1	-	-	-	-	-	-
-	-	Water	-	-	-	-	-	-	-	3	3	1
-	-	Relative humidity	1	1	1	2	1	1	1	3	3	1
Pollution	Tightness	Pollution	-	-	-	-	-	1	-	-	1	-
Mains	Circuit	Voltage	1	1	1	3	2	-	1	1	1	1
Cosmic	Circuit	Voltage	1	-	-	-	-	-	-	-	-	-
Mounting	Mechanical	Chock/ vibration	1	-	-	1	1	1	1	-	-	1
LASJ: large-area solder joint, MLCC: multilayer ceramic capacitor, IC: integrated circuit, Cap.: capacitor Level of importance: 3(high)<->1(low)												

Table 25: Impact of ST architecture on the number of components.

No. of power stage	No. of power semiconductor	No. of DC-link capacitor	No. of winding components	No. of gate driver circuit	System reliability
1 stage	Low	Low	Low	Low	High
2 stage	Medium	Medium	Medium	Medium	Medium
3 stage	High	High	High	High	Low

Evaluating the reliability of the ST requires taking into account all single components (e.g. transformers, power semiconductors, drivers, cooling equipment etc.) and their reliability, which is out of the scope of this report. However, the number of the power conversion stages has an impact on the number of components in the system. Therefore, the architectures are categorized by the number of power stages as shown in **Table 25**. Remarkably, this does not necessarily have an impact on the reliability, because the reliability is dependent on the quality of the single device. Moreover, a higher number of components enables to include redundancy on a lower level (e.g. building block level instead of system level) and enables to implement fault tolerance. Apart from the material costs to obtain redundancy in the system, the redundancy has an impact on the efficiency. In a modular medium voltage converter, this was demonstrated for traction applications, where the redundancy form *n=8* to *n=9* reduced the efficiency [58].

4.2.3. Reliability of power semiconductors

As reported in the industry survey, power semiconductors are among the most sensitive components in power converters. For this reason, this subsection reviews the common failure mechanisms and the lifetime model for these devices. The wear-out based failure mechanisms of power semiconductors are highly dependent on the temperature. On the one side, the operation with high temperature is limiting the lifetime and on the other side, it thermal cycles reduce the lifetime. The thermal swing is critical for most failures of power modules [60]. It is affecting thermo-mechanical stresses at the interconnections of layers with different materials with different coefficients of thermal expansion. The wire bonded scheme of power module with the Direct Bonded Copper (DBC) is shown in **Figure 82**, highlighting the common failures such as chip solder fatigue, bond wire lift off and baseplate solder fatigue [59].

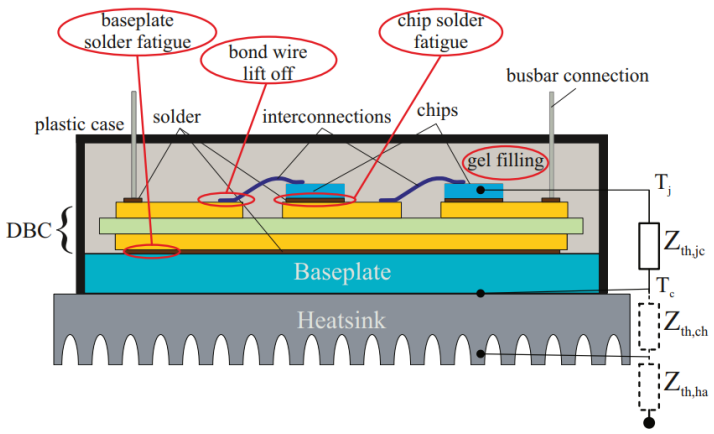


Figure 82: Scheme of a power electronic module with heatsink, common failures and thermal impedances [59].

Furthermore, for protection against corrosion and environmental influences, a gel filling immerses the module to guarantee dielectric strength. The main aging processes of the silicone gel are water trees, partial discharge and electrical trees, which are degrading effects causing aging but not the immediate destruction [61].

The PoF approach can be employed for a lifetime prediction of power semiconductor [60]. The failure mechanisms for bond wire lift off can be modelled by expressing the number of thermal cycles to failure N_f in dependence of the mean temperature $T_{j,mean}$ and the magnitude of the thermal swing ΔT in (36).

$$N_f = a_1 \cdot (\Delta T)^{a_2} \cdot e^{\frac{a_3}{T_{j,mean}+273°C}} \tag{36}$$

Thereby, a_1, a_2, and a_3 are fitting parameters. This lifetime model is visualized in **Figure 83**, where the relation between the thermal stresses and the lifetime is identified. The lifetime is related to the number of thermal cycles to failure, with exponential influence of the magnitude ΔT and the average junction temperature during the cycle $T_{j,mean}$.

As a limitation of this lifetime model, only a single magnitude for the thermal swing is considered, which is not practical for a system operating with a real profile. Hence, a cycle counting method is required to decompose the temperature profile and to determine all thermal cycles in a temperature profile. For this purpose, the rainflow counting algorithm is widely employed for fatigue analysis [63]. Subsequently, Miner's rule can be applied to calculate the accumulated damage from all thermal cycles in the profile.

$$D_{acc} = \sum \frac{N_i}{N_{fi}} \tag{37}$$

In this equation, D_{acc} is the accumulated damage, N_i the number of detected cycles in the i-th stress range, and N_{fi} the number of cycles to failure of the i-th stress range. When the accumulated damage becomes one, the device fails.

As a way to influence the lifetime of the devices, the maximum junction temperature can be designed for lower maximum temperatures. This can be achieved with a powerful cooling system achieving low thermal resistances. Apart from the reduction in thermal stress, this has the advantage to increase the maximum current conduction capability of the power semiconductors.

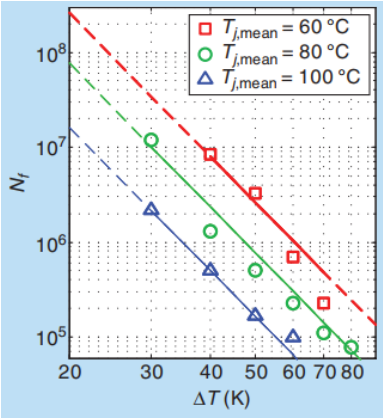


Figure 83: The number of cycle to failure and the relationship between thermal swing and cycles to failure [62].

4.2.4. Reliability of capacitors

The second component identified in the survey to be sensitive are the capacitors. Their failure mechanisms are dependent on the employed technology, whereby the frequently used technologies are Aluminum Electrolytic Capacitors (Al-Capacitors), Metallized Polypropylene Film Capacitors (MPPF-capacitors) and Multi-Layer Ceramic Capacitors (MLC-capacitors). The major failure mechanisms presented in literature [64, 65, 66] for Al-Caps, [67, 68, 69][for MPPF-Caps and [70, 71, 72] for MLC-Caps, are summarized in Table 26, describing the failure modes, failure mechanisms and corresponding critical stressors.

The most widely used empirical lifetime model for capacitors is shown in (38) and describes the influence of temperature and voltage stress on the lifetime of the capacitor.

$$L = L_0 \cdot \left(\frac{V}{V_0}\right)^{-n} \cdot exp\left[\left(\frac{E_a}{K_B}\right)\left(\frac{1}{T} - \frac{1}{T_0}\right)\right] \quad (38)$$

Thereby, L is the lifetime, L_0 is the lifetime under testing conditions, V is the applied voltage, V_0 is the voltage under testing conditions, T is the hotpot temperature and T_0 is the temperature under testing conditions. E_a is the activation energy, K_B the Boltzmann's constant (8.62 × 10−5 eV/K), and n is the voltage stress exponent.

Table 26: Summary of failure modes, critical failure mechanisms and stressors [21].

Type	Failure modes	Critical failure mechanisms	Critical stressors
Al	Open circuit	Self-healing dielectric breakdown	V_C, T_a, i_C
		Disconnection of terminals	Vibration
	Short circuit	Dielectric breakdown of oxide layer	V_C, T_a, i_C
	Wear-out	Electrolyte vaporization	T_a, i_C
		Electrochemical reaction	V_C
MPPF	Open circuit	Self-healing dielectric breakdown	V_C, T_a, dV_C/dt
		Connection instability by heat contraction of a dielectric film	T_a, i_C
		Reduction in electrode area caused by oxidation of evaporated metal due to moisture absorption	Humidity
	Short circuit	Dielectric film breakdown	V_C, dV_C/dt
		Self-healing due to overcurrent	T_a, i_C
		Moisture absorption by film	Humidity
	Wear-out	Dielectric loss	V_C, T_a, i_C, Humidity
MLC	Short circuit	Dielectric breakdown	V_C, T_a, i_C
		Cracking, damage to capacitor body	Vibration
	Wear-out	Oxide vacancy migration, dielectric puncture, insulation degradation, micro-crack within ceramic	V_C, T_a, i_C, Vibration
* V_C: capacitor voltage, i_C: capacitor ripple current, T_a: ambient temperature.			

Table 27: Testing samples of DC film capacitors [42].

Testing samples	Testing condition
Group 1 – 1100V/40uF (10 pcs)	85 °C and 85% RH
Group 2 – 1100V/40uF (10 pcs)	85 °C and 70% RH
Group 3 – 1100V/40uF (10 pcs)	85 °C and 55% RH

* RH: Relative Humidity

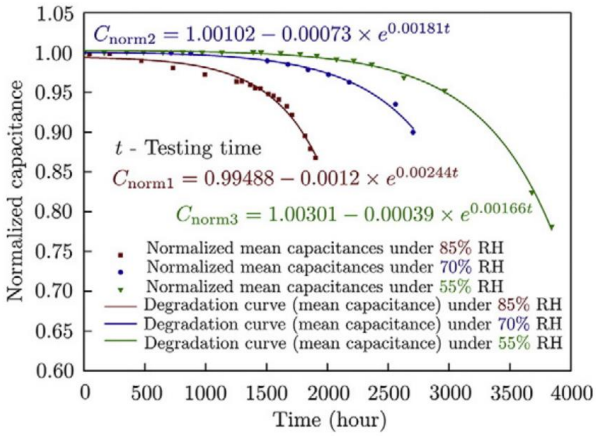


Figure 84: Normalized capacitances and the corresponding degradation curves under different humidity levels [73].

During these tests, the capacitance was sampled at 100 Hz and the capacitances are normalized by initial value of each sample. This test was performed with three different humidity levels as shown in **Figure 84**. As it can be seen, a higher humidity reduces the useful lifetime of the capacitors.

For preventing failures of capacitors, a suitable design under consideration of the target lifetimes is of importance. The trial side should be considered as well to take into account the humidity and the ambient temperature.

Apart from the temperature, the humidity was shown to be a stressor for MPPC capacitors. To address this problem, in [42], the influence of the relative humidity on the reliability of film capacitors was investigated under the test condition shown in **Table 27**.

4.2.5. Failure of the cooling system

The cooling system is needed to dissipate the losses and to prevent system failures caused by over-heating. Components, which are commonly cooled are power semiconductors, capacitors and inductors. Thus, the reliability of the cooling system needs to be considered to evaluate the system reliability. Furthermore, once a failure occurs in the cooling system, the power conversion capacity of power converters may decreased, because the system will undergo overheating, which will result in intermittent failures and catastrophic failures.

As a case study [74], the reliability of each sub-component in an offshore wind power converter was assessed. This yields to the result shown in **Figure 85**, where the control system (35%) was found to be most critical, followed by the semiconductors (25%) and the cooling system (18 %).

For analysing the reliability of the cooling system, the cooling technology employed in high power wind turbines was categorized and evaluated as shown in **Table 28** [75].

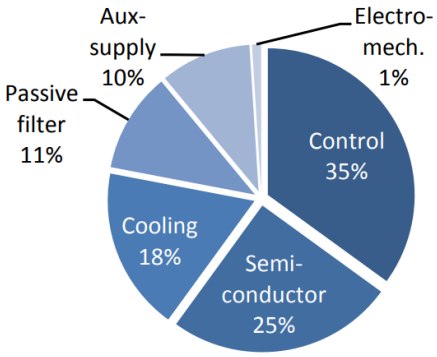


Figure 85: Failures in an offshore wind power generation system [74].

Table 28: Comparison of several cooling technology in wind turbine [75].

Cooling technology	Cooling medium	cost	Cooling capacity	Service life	Cooling efficiency
Air-air	air	low	Small (<300kW)	short	low
Liquid-air	Lubricating oil	low	Medium (>300kW)	medium	medium
Air-liquid-air	antifreeze	medium	medium	medium	high
Centralized cooling	Water or air	high	big	long	medium

4.2.6. Interaction of the ST's component with the ambient conditions

The ST is expected to fit into the substation of a conventional transformer and to be enclosed to be protected from harsh environments such as dust, rain and climate change. However, the components inside the ST-substation generate losses, which increases the temperature inside the enclosure. This increase of the temperature can potentially reduce the lifetime of components. Consequently, the temperature of the ST has to be kept within a safe operating range [76].

Apart from the temperature inside the ST-substation, the condensation is another important aspect, which can reduce the lifetime of components, such as capacitors and power semiconductors. For power semiconductors, the condensation has an impact on the electric field at the periphery of the power semiconductors, which is increasing the stress and thereby reduces the lifetime [76]. Moreover, the modules are not hermetically sealed, which allows moisture to permeate into the module. The diffusion of the moisture reduces the blocking voltage and affects power semiconductor corrosion [77].

To prevent the negative effects, the root cause of condensation needs to be understood and can be explained with the following points [77]:

- Changes in relative air pressure: an increase in pressure on a sealed system causes an increase of the relative humidity.
- Changes in relative air temperature: a drastic change in temperature can affect conditions, where the component temperature falls below the dew point. This temperature change may occur by changing the system operation and climate change during the transition between day and night.

For the mitigation of condensation, the following solutions can be applied [77]:

- Cabinet heater: increasing the temperature within the substation decreases the relative humidity for a fixed absolute humidity.
- Coolant temperature control in case of liquid cooled system: the coolant temperature should be kept above the temperature within the substation to prevent the temperature of components to drop below the dew point.
- Fan control in case of air-cooled system: in the same manner of the coolant temperature control, the fan speed is controlled to keep the heatsink temperature above the dew point.
- Dehumidifiers: the moisture from the air is directly removed.

4.3. Modularity impact on the reliability

The discussion about the impact of the modularity on the reliability is a controversial discussion. On the one hand, a high degree of modularity increases the number of components, which can possibly fail. On the other hand, fault tolerance requires a certain redundancy in the system. This redundancy can be implemented on different levels in the modularity, e.g. system level, converter level or building block level. The potential choice of the modularity level has an impact on the additional costs, the complexity of the hardware and the complexity of the controller implementation. As it can be seen in **Table 29**, this results in a conflicting goal between additional costs and the complexity to achieve redundancy in the system.

Table 29: Opportunities of modularity in different levels of the ST.

Modularity level (system, topology or cell)	Additional cost	Complexity
Cell/building block	Low	High
Topology	Medium	Medium
System	High	Low

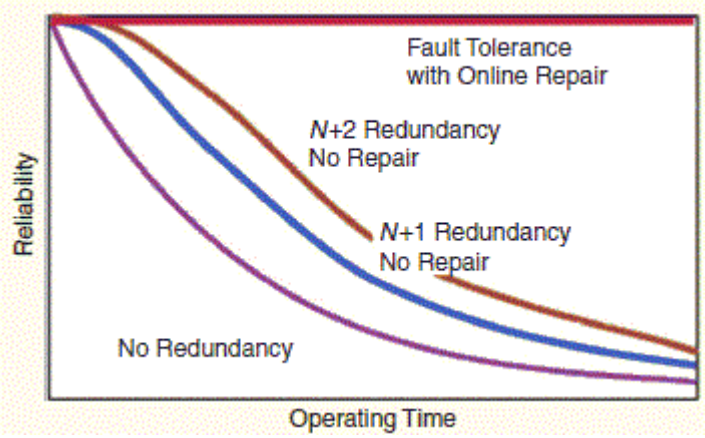


Figure 86: Impact of redundancy on the reliability of a system [78].

For the visualization of the general impact of redundancy, **Figure 86** shows the impact of redundancy on the reliability in a repairable system. One redundant part/system enables to increase the reliability significantly and in case online repair is possible, the system can be operated without interruption.

Devices of the ST may fail without prior detection of a monitoring system. In case of a non-modular power converter without redundancy, this results in the outage of the ST and the disconnection of the grids. This is not desired and therefore, it is recommended to

1) Implement a protection system for the ST, which enables to isolate failures within the ST
2) Implement redundancy on an arbitrary level, which covers all stages of the ST.

The implementation of the protection system for fault isolation is recommended to minimize the impact of a fault on other devices in the system and thereby minimize the damage of the fault. The redundancy on each level is recommended to ensure the continuous operation. In the MV-side, this is expected to be a series connected building block or a parallel converter on the system level. In the LV-side this can be realized with a parallel converter, redundancy on the phase level of redundancy on the device level.

4.4. Innovative solution for reliability enhancement

This section provides potential opportunities to increase the reliability of the ST. Based on the identified most sensitive components, power semiconductors and capacitors, condition monitoring techniques are discussed and potential control based solutions to reduce the stress for these components are suggested.

4.4.1. Condition monitoring

A possibility for the prediction of a failure before its occurrence is real time monitoring of the device, referring to condition monitoring. Commonly, parameters are identified, which correlate with the wear-out and a failure criterion is defined for the determination of the end of life.

For power semiconductors, it is suggested in literature to monitor the thermal resistance between junction and case for prediction of solder fatigue [79]. For the prediction of bond wire lift off failures in IGBTs, the collector-emitter voltage is proposed to be monitored and for MOSFETs the on increase during the lifetime [80]. The detection of the junction temperature is another way to monitor the wear-out. Possible ways of monitoring the junction temperature without direct measurement are the measurement of the derivative of the collector current, the short circuit current or model based approaches [79, 80, 81].

Similar like condition monitoring for power semiconductors, the condition of capacitors can be monitored. In general, the capacitance of capacitors reduces over time. For the commonly applied Al-Caps, the Equivalent Series Resistance (ESR) increases over time. The typical end-of-life criteria and degradation precursors for three types of capacitors are described in **Table 30**.

Table 30:Typical end of life criteria and condition monitoring parameters for capacitors [82].

	Al-Caps	MPPF-Caps	MLC-Caps
Failure criteria	C: 20% reduction ERS: 2 times	C: 5% reduction DF: 3 times	C: 10% reduction R_p>$10^7\Omega$ DF: 2 times
Degradation precursors	C or ESR	C	C, R_p
* DF: Dissipation Factor, R_p: insulation resistance			

4.4.2. Power semiconductors

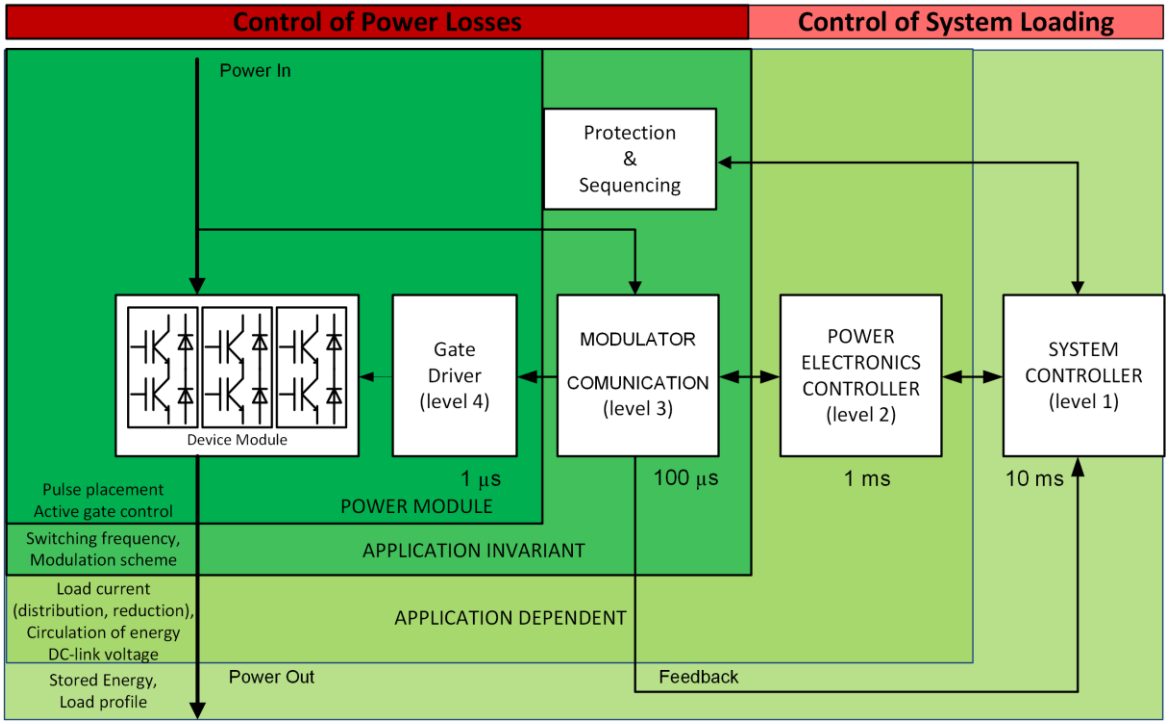


Figure 87: various chances for the implementation of active thermal control in a power electronic system [83].

As discussed before, the thermal stress is the main killer for power semiconductors and a reduction of the thermal stress enables an extension of the lifetime. Apart from the opportunities in the system design (power semiconductor choice, cooling system design, topology choice), there is the potential to use the control of the system to reduce thermal stress and thereby increase the lifetime of the system. This is referred to as active thermal control and in the following a short review is given on the topic. In general, active thermal control can be grouped into the control of the power losses and into the control of the system loading. The applicability is thereby dependent on the system design and a higher degree of redundancy enables a higher potential to control the thermal stress for the devices. On the system level, there is the possibility to reduce the load current (level 1), to share the power between paralleled devices or systems (level 2), to modify the loss distribution (level 3) or to displace pulses with an intelligent gate driver (level 4). These approaches can be applied independently from each other in different time ranges, which are visualized in **Figure 87**.

A particular active thermal control algorithm, referred to as power routing, utilizes potentially available redundancy and routes the power with the goal to control the stress of series-connected or parallel-connected building blocks. This concept is visualized in **Figure 88**, which shows a modular system based on three building blocks. In **Figure 88** (a) the power p_1, p_2 and p_3 are processed equally by the building blocks 1, 2 and 3, respectively, whereas in **Figure 88** (b), the sharing of three series connected building blocks is controlled and in **Figure 88** (c) the sharing among parallel connected building blocks is controlled. This can be used to control the thermal stress and influence the failure mechanisms, which are dependent on the processed power.

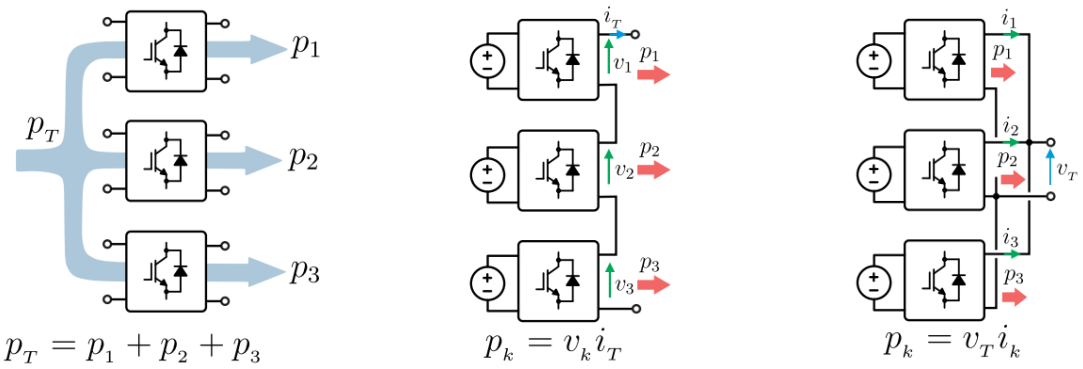


Figure 88: (a) power routing concept in a modular system. (b) Series connection of building blocks, where the voltage is used to control the power and (c) parallel connection of the building blocks, where the current is used to control the power [84].

The power routing concept is illustrated in Figure 89. As an example, a system based on three building blocks connected in parallel is shown in Figure 89 (a). In this system, each building block has an expected remaining lifetime defined by λ_1, λ_2 and λ_3 for the building blocks 1, 2 and 3, respectively. In the example shown in Figure 89 (a), the remaining lifetime for the building block 1 is shorter than the remaining lifetime of the other building blocks. This means that building block 1 is closer to its end of life than the other ones. Once it reaches the end of life, the entire system operation will be interrupted. Therefore, to extend the remaining useful lifetime of the entire system, it is proposed to increase the lifetime of building block 1. One strategy to increase the lifetime of the power modules in the building blocks is to reduce the operation temperature of the power semiconductors. This is illustrated in Figure 89 (b), where initially all building blocks process the same power. This is resulting in similar operation temperatures, but the building block 1 has a shorter remaining useful lifetime. By means of the power routing, the processed power of building block 1 (p_1) can be reduced in order to reduce its temperature within the power modules, as shown in Figure 89 (b). As a result, the expected lifetime of building block 1 and, consequently, the lifetime of the entire system is increased. Of course, the power processed by the building blocks 2 and 3 will increase, as well as the temperature within the respective power modules. Although the expected lifetime of the modules 2 and 3 is slightly reduced, the lifetime of the system is increased. Thus, this example has shown, that it is possible to delay the time to the next failure and therefore improve the availability of the system by means of the power routing.

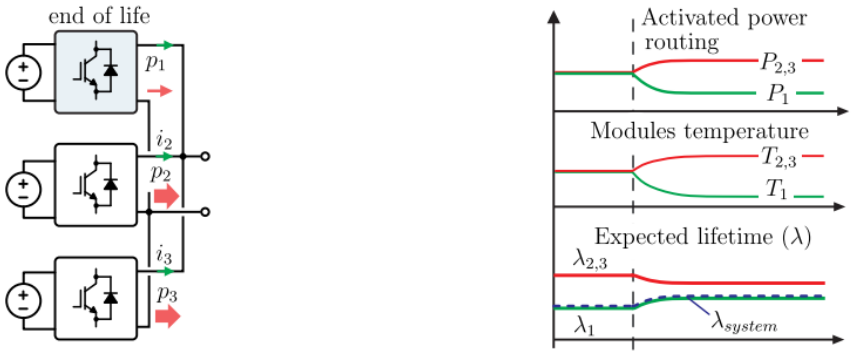


Figure 89: Example of power routing impact on the lifetime: (a) block diagram of an example system highlighting one module is close to the end of life, (b) expected lifetime graphic showing the impact of the power routing on the system's lifetime.

4.4.3. DC-link capacitors

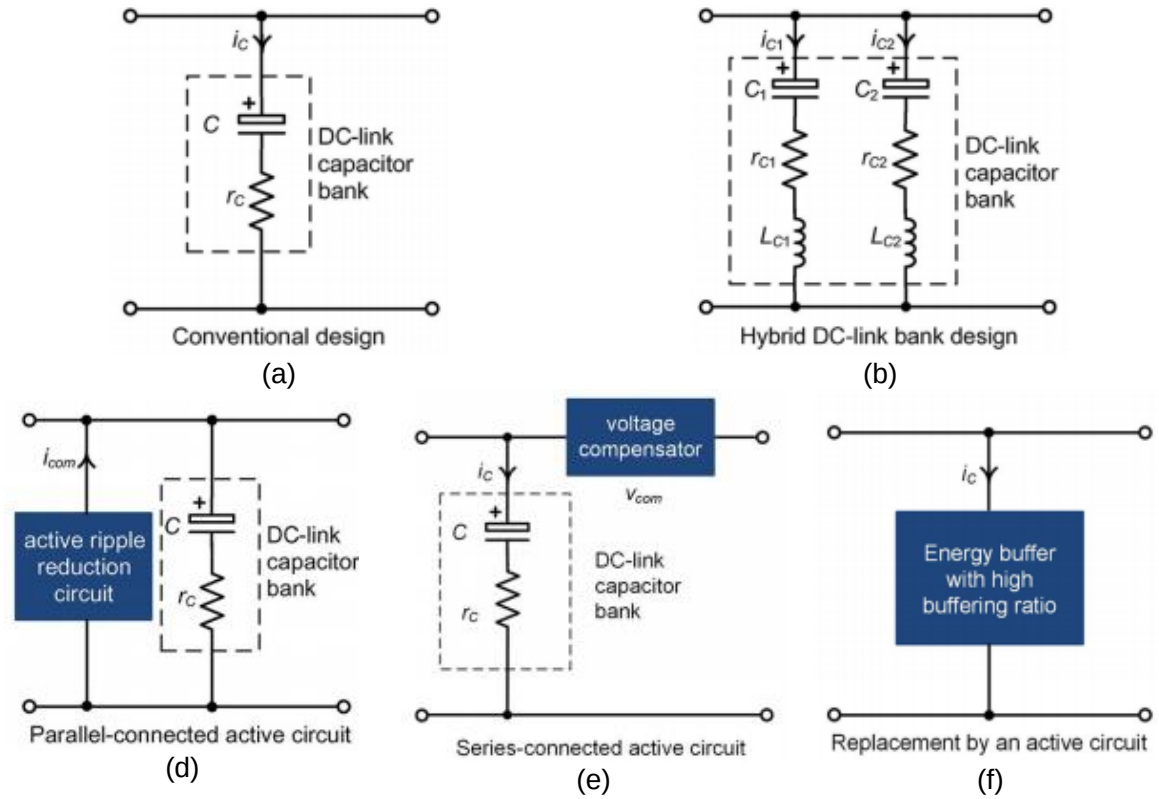


Figure 90: dc-link design solutions [82].

The design of the DC-links in a ST is another challenge in minimizing the costs on the one and to provide the required performance on the other hand. The potentially applicable solutions can be categorized as shown in **Figure 90**.

The most widely used solution is to employ one type of capacitor with consideration of characteristics of the chosen capacitor as shown in **Figure 90** (a). To utilize the characteristics of different type of capacitors, a hybrid design solution is proposed as shown in **Figure 90** (b). In [85], the effect of the hybrid solution was shown to reduce the ripple current stress of electrolytic capacitors by employing electrolytic capacitor and film capacitor together.

Figure 90 (d) and (e) show the concept employing an additional ripple power port connected in either parallel [86] or series [87]. The advantage of series solution is that the required power capacity of the ripple port can be much lower compared with that of parallel solution. Finally, the conventional DC-link capacitors can be directly replaced by an energy buffer as shown in **Figure 90** (f) [88].

The active DC-link solutions in **Figure 90** (d)-(f) provides the opportunities to reduce the size of the DC-link capacitors, but introduce additional circuits and its control schemes.

4.5. Operation and Maintenance concepts

The implementation of operation and maintenance concepts is widely employed in power electronics applications. However, the metrics for an electric drive, a wind turbine and an ST are expected to be different, because the costs for unplanned down time are expected to be significantly higher for the ST. Therefore, the figure of merits is expected to change completely and result in a different system design and component sizing. However, as an application, where

operation and maintenance concepts are applied for a long time, the wind energy sector is identified. Unfortunately, manufacturers share only limited information about failures and availability of their wind turbines. One of the few published reports about operation and maintenance is highlighting the trade-offs and challenges in the maintenance planning [89]. First, it is distinguishes between scheduled and unscheduled maintenance. Scheduled maintenance targets to refurbish components with a specified lifetime before their failure. Usually, the costs for scheduled maintenance can be determined well in advance. Unscheduled maintenance instead needs to be scheduled in case of an unexpected outage of the system. The costs for the unexpected maintenance may be very high and a suitable supply chain needs to be determined to limit delays.

The same report [89] identifies potentials for reducing costs by increasing the reliability and reducing maintenance costs. The reliability increase is suggest to be achieved with the identification of critical components and characterization of their failure modes as well as the determination of the root cause for the failure. The reduction of the maintenance costs is suggested to be achieved through the development of a logistic plan, the identification of opportunities for redundancy, improved training for the employees to perform effective failure and root cause analysis. Finally, the implementation of a condition monitoring system is recommended.

By applying the recommendations for the application of the ST in the distribution grid, it is recommended to request the following information:

- Maintenance plan including the costs
- Information about the time to the next repair and a supply chain for the repair parts
- Information about potentially applied monitoring system
- Potentially innovative operation and maintenance concepts

4.6. Environmental impact of the ST

The cooling system for the devices within the ST may include liquids, which are hazardous for the environment. These liquids may be glycol, oil or others and may require protection according to the British regulations.

4.7. Safety requirements for STACOM application

In addition to the reliability analysis, which has been provided, the requirements from a tender for a STATCOM is considered [90]. A selection of important requirements are listed in the following:

- Continuous monitoring and data logging of the waveforms (voltage, current and figure pulses) with high frequency and slow data logging (50 Hz) of the control and power system quantities
- Alarms and trips in case of a failure, remote reset facilities
- Protection of the components as shown in **Table 31**
- Cooling system requirements
    - Shall be rated to maintain full power capacity and to be simple, reliable and easy to maintain with a minimum number of sensors
    - Redundancy for pumps and replacement of faulty parts without interruption of the STATCOM operation
    - 50.000 hours of operation without maintenance

  - Lifetime of the cooling system should comply to the lifetime of the STATCOM
  - The quantities required at least to be monitored are shown in **Table 32**.
- Warranty, reliability and availability
  - Design life of 40 years; secondary equipment design life of 20 years
  - Five years warranty
  - More than 4000 h between unplanned outages
  - Availability of 99.5 % (per year)

Several of these recommendations can be adopted for the ST. However, 4000 h (less than half a year) until the first unplanned outage may to be low and a higher time period can be requested.

Table 31: Protection requirements for STATCOM.

Component	Protection
Power converter	Instantaneous overcurrent, time overcurrent, under voltage, overvoltage, temperature supervision, reverse phase lockout supervision, ground fault supervision
Reactors	Overcurrent, earth fault
Capacitors	Overcurrent and earth fault, overload, unbalance, neutral unbalance, under frequency.

Table 32: Alert level depending on failure type in cooling system.

Air-cooled system		Liquid-cooled system	
Alert	Failures	Alert	Failure
Alarm	• Blower transfer • High exhaust air temperature or high heat sink temperature • High differential pressure across the filter • Low air flow	Alarm	• Depleted de mineralised cell if high resistivity is required • Low water sensitivity if high resistivity is required • Low coolant level • Primary pump stopped • Primary fan stopped • High coolant temperature • Failure of pump cycling scheme • Leak detected
Trip	• Excessive exhaust air temperature or high heat sink temperature • Loss of air flow	Trip	• Extra high temperature • Extra low coolant level • Pumps stopped or blocked flow

5. Key findings and recommendations

This report has address the hardware design for the ST, software design for the ST and reliability of the ST. Based on the three sections, key findings and recommendations are listed in the following.

5.1. Findings and recommendations for the hardware

- A comparison of potential ST architectures has been made and the applicability in the LV Engine schemes is evaluated. Most of the considered topologies have been found to be capable to provide services by means of reverse power flow capability, reactive power control and DC-connectivity. It is concluded, that the availability of at least one DC-link is recommended in order to ensure a minimum level of decoupling of the two AC sides.

- In the topology comparison, the isolation stage has been found to be the most critical stage, which may be the bottleneck for obtaining high efficiency of the system. For limiting the stress of the inductive components, high-voltage and high-frequency operation have discussed to be critical and it is recommended to apply modular topologies for reducing the stress of the components.

- For the applicability of fault tolerance, redundancy of the different architectures is evaluated on different levels, such as system level, topology level and building block level. It is recommended to apply redundancy on one of the levels in combination with fault-tolerance concepts.

- Different power semiconductor technologies have been discussed for the applicability in the three stages of the ST. Because of the lower costs, Si-IGBTs have been preferred in the AC stages, whereas SiC-MOSFETs would be preferred in the isolation stage to guarantee an acceptable efficiency.

- Based on commercially available power converters, the efficiency of the LV-stage is expected to be higher than 98%. Commercially available medium voltage converters have a high efficiency range, whereas some of them achieved 99% of efficiency. The isolation stage holds uncertainty and will result in a trade-off between system costs and efficiency.

- Different cooling systems have been discussed, namely air-cooling and water-cooling systems for the applicability in the ST. Advantages for the volume have been demonstrated for water-cooled systems and the impact of the device utilization in dependence of the cooling system performance was demonstrated.

- The behaviour of the ST and the resulting losses along with their impact on the minimum sizing of the power semiconductors have been derived. It is highlighted that the overcurrent which the power converter can tolerate in continuous conduction mode (for example in case of a fault to let the protections intervene with the right selectivity) is related to the conduction losses and chosen cooling system and consequently is not directly to be associated to the rated current in normal operation or to the overcurrent which the power converter may be requested to control (hence switching) during transients.

5.2. Findings and recommendations for the software

- For different ST architectures, the control variables have been defined in the different LV Engine schemes. Grid feeding control and grid forming control have been introduced and both control modes are required to be implemented in AC-connected converters of the ST.

- Seamless transfer between the grid-feeding and grid-forming control without interruption and without violating the grid codes is required.

- In the grid feeding operation, the controller is required to compensate low order harmonics of the output current with the 5th, 7th, 11th and 13th order. A grid synchronization mechanism is required, which is able to track the phase during grid faults and is able to separate positive and negative sequence of the fundamental grid voltage.

- The integration of a DC-grid is recommended to be done by means of a connection to the LVDC-link and it is requested to control the LVDC-grid voltage within 90-110% of the nominal grid voltage.

- The controller should be able to control the frequency within the range of 47 Hz to 52 Hz.

- The control system of the ST is required to have suitable communication interfaces for the data exchange with Smart Meters and Smart Control Units. Within the Smart Control Units, the reference generation for the voltage setpoints (in grid forming control) and the power references (in grid-feeding control) need to be generated. The control of the voltage/current instead is expected to be implemented on the substation level.

5.3. Findings and recommendations for the reliability

- In various power electronics applications, power semiconductors and capacitors have been identified to be critical components for the reliability. Their failure mechanisms and stressors are reviewed and opportunities to overcome problems in the system design are evaluated. The devices should be designed for the lifetime of the ST and health monitoring for the sensitive components is welcome for device monitoring.

- Redundancy is recommended to be implemented for increasing the reliability and it is required to be implemented in such a way, that the system can continue to operate after the failure of a redundant part. The measures for reliability and availability should include the relevant failure definitions and scoring criteria applied as well as a description of their reliability organization and reporting structure.

- Manufacturers should provide operation and maintenance concepts for the determination of the operation of the ST and determine time intervals for the maintenance and the related costs. The time to repair for unplanned failures should be defined as well as a supply chain for the repair parts, which need to be available for the whole lifetime of the ST. Innovative operation and maintenance concepts with the goal to provide high reliability are welcome.

6. Conclusions

This report has investigated through detailed literature research the Smart Transformer requirements with respect to the hardware, software and reliability. An overview has been provided on the design of the ST by means of potential designs, related power converter topologies, power semiconductors, the cooling system and the medium frequency transformer. For the ST architecture, it is recommended to have at least on dc-link for the isolation of disturbances in the grids. The dc-grid is recommended to be connected through an isolated dc/dc converter to obtain galvanic isolation for the isolation of the different grids. The power semiconductor choice will be a trade-off between costs and performance, whereas new power semiconductor technology, like Silicon Carbide is suitable for the stage, which employs the isolation. The rating of the power semiconductors shall take into account the trial site with the grid protection and the rules for the grid connection, like the British G99.

The report has addressed the control and communication capability of the ST and the concepts for the controller design, including coordinate transformation, grid synchronization, specific control schemes, hardware for the controller, controller implementation and communication protocols. The ST requires the capability to operate in grid feeding (power) control and grid forming (voltage) control, whereby a seamless change of the control objectives is required. The grid synchronization requires to be fast and requires to continue to operate even during grid faults. For the implementation of an intelligent control grid for the grid optimization, suitable communication protocols need to be installed.

The concept of reliability and availability have been introduced and discussed for ST applications. It is recommended to request from the manufacturers to provide solutions with high reliability and availability and to quantify there claimed measures. Condition monitoring systems are desired to enable health monitoring of the system and the termination of prognostic maintenance. Moreover, it is recommended to request detailed operation and maintenance plans with supply chains for the provision of repair parts.

7. References

[1] SP Energy Networks. LV Engine project. [Online]. Available: https://-www.spenergynetworks.co.uk/pages/lv_engine.aspx

[2] J. Burkard and J. Biela, “Evaluation of topologies and optimal design of a hybrid distribution transformer,” in *2015 17th European Conference on Power Electronics and Applications (EPE’15 ECCE-Europe)*, Sept 2015, pp. 1–10.

[3] S. Bala, D. Das, E. Aeloiza, A. Maitra, and S. Rajagopalan, “Hybrid distribution transformer: Concept development and field demonstration,” in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2012, pp. 4061–4068.

[4] R. P. Kandula, H. Chen, A. Prasai, F. Lambert, J. Schatz, and D. Divan, “Field upgradeable transformer: A fractionally-rated voltage regulator for the distribution system,” in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2016, pp. 1–8.

[5] R. P. Kandula, A. Iyer, R. Moghe, J. E. Hernandez, and D. Divan, “Power router for meshed systems based on a fractionally rated back-to-back converter,” *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5172–5180, Oct 2014.

[6] J. E. Huber and J. W. Kolar, “Volume/weight/cost comparison of a 1mva 10 kv/400 v solid-state against a conventional low-frequency distribution transformer,” in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2014, pp. 4545–4552.

[7] F. Bignucolo, M. Bertoluzzo, and C. Fontana, “Applications of the solid state transformer concept in the electrical power system,” in *2015 AEIT International Annual Conference (AEIT)*, Oct 2015, pp. 1–6.

[8] H. Chen and D. Divan, “Design of a 10-kv -kva soft-switching solid-state transformer (s4t),” *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5724–5738, July 2018.

[9] L. F. Costa, G. D. Carne, G. Buticchi, and M. Liserre, “The smart transformer: A solid-state transformer tailored to provide ancillary services to the distribution grid,” *IEEE Power Electronics Magazine*, vol. 4, no. 2, pp. 56–67, June 2017.

[10] K. Basu, A. Shahani, A. K. Sahoo, and N. Mohan, “A single-stage solid-state transformer for pwm ac drive with source-based commutation of leakage energy,” *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1734–1746, March 2015.

[11] N. Hugo, P. Stefanutti, M. Pellerin, and A. Akdag, “Power electronics traction transformer,” in *2007 European Conference on Power Electronics and Applications*, Sept 2007, pp. 1–10.

[12] F. Fang and Y. W. Li, “Modulation and control method for bidirectional isolated ac/dc matrix based converter in hybrid ac/dc microgrid,” in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct 2017, pp. 37–43.

[13] Q. Zhu, L. Wang, D. Chen, L. Zhang, and A. Q. Huang, “Design and implementation of a 7.2kv single stage ac-ac solid state transformer based on current source series resonant converter and 15 kv sic mosfet,” in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct 2017, pp. 1288–1295.

[14] J. E. Huber, D. Rothmund, and J. W. Kolar, “Comparative evaluation of isolated front end and isolated back end multi-cell ssts,” in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, May 2016, pp. 3536–3545.

[15] M. Steiner and H. Reinold, “Medium frequency topology in railway applications,” in *2007 European Conference on Power Electronics and Applications*, Sept 2007, pp. 1–10.

[16] C. Zhao, D. Dujic, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti, “Power electronic traction transformer - medium voltage prototype,” *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3257–3268, July 2014.

[17] J. E. Huber and J. W. Kolar, “Solid-state transformers: On the origins and evolution of key concepts,” *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 19–28, Sept 2016.

[18] J. Taufiq, “Power electronics technologies for railway vehicles,” in *2007 Power Conversion Conference - Nagoya*, April 2007, pp. 1388–1393.

[19] R. Raju, M. Dame, and R. Steigerwald, “Solid-state transformers using silicon carbide-based modular building blocks,” in *2017 IEEE 12th International Conference on Power Electronics and Drive Systems (PEDS)*, Dec 2017, pp. 1–7.

[20] H. Chen and D. Divan, “Soft-switching solid-state transformer (s4t),” *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 2933–2947, April 2018.

[21] M. Liserre, “The smart transformer: impact on the electric grid and technology challenges,” iEEE eT&D 2017 IEEE Workshop on Electronic Power Transmission and Distribution.

[22] M. K. Das, C. Capell, D. E. Grider, S. Leslie, J. Ostop, R. Raju, M. Schutten, J. Nasadoski, and A. Hefner, “10 kv, 120 a sic half h-bridge power mosfet modules suitable for high frequency, medium voltage applications,” in *2011 IEEE Energy Conversion Congress and Exposition*, Sept 2011, pp. 2689–2692.

[23] A. Q. Huang, “Medium-voltage solid-state transformer: Technology for a smarter and resilient grid,” *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 29–42, Sept 2016.

[24] D. Li, C. N. M. Ho, L. Liu, and G. Escobar, “Reactive power control for single-phase grid-tie inverters using quasi-sinusoidal waveform,” *IEEE Transactions on Sustainable Energy*, vol. 9, no. 1, pp. 3–11, Jan 2018.

[25] O. Deblecker et al., “Comparative Study of Optimal Designed DC-DC Converters with SiC and Si Power Devices,” Advanced Silicon Carbide Devices and Processing, IntechOpen, 2015.

[26] F. . P. C. . C. G. Fraunhofer Institute for Solar Energy Systems, “Photovoltaics report,” *https://www.ise.fraunhofer.de/content/dam/ise/de/documents/publications/studies/Photovoltaics-Report.pdf*, 2018.

[27] L. F. Costa, G. Buticchi, and M. Liserre, “Efficiency/cost trade-off design of a multiple-active-bridge converter for smart transformer,” in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 1163–1170.

[28] A. da Silva Dias, D. B. Cândido, A. P. Almeida, and J. A. Alves, “Cooling methods design for power electronics converters,” in *2017 Brazilian Power Electronics Conference (COBEP)*, Nov 2017, pp. 1–6.

[29] U. Drofenik, G. Laimer, and J. W. Kolar, “Theoretical converter power density limits for forced convection cooling,” in *Proceedings of the International PCIM Europe Conference (PCIM 2005)*, 2005.

[30] ——, “Pump characteristic based optimization of a direct water cooling system for a 10-kw/500-khz vienna rectifier,” *IEEE Transactions on Power Electronics*, vol. 20, no. 3, pp. 704–714, May 2005.

[31] B. J. Lyons, J. G. Hayes, and M. G. Egan, “Magnetic material comparisons for high-current inductors in low-medium frequency dc-dc converters,” in *APEC 07 - Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition*, Feb 2007, pp. 71–77.

[32] T. Guillod, R. Färber, F. Krismer, C. M. Franck, and J. W. Kolar, “Computation and analysis of dielectric losses in mv power electronic converter insulation,” in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2016, pp. 1–8.

[33] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, “Overview of control and grid synchronization for distributed power generation systems,” *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1398–1409, Oct 2006.

[34] R. Teodorescu, F. Blaabjerg, and M. Liserre, “Proportional-resonant controllers: A new breed of controllers suitable for grid-connected voltage-source converters,” *Journal of Electrical Engineering*, 2017.

[35] V. M. Moreno, M. Liserre, A. Pigazo, and A. Dell’Aquila, “A comparative analysis of real-time algorithms for power signal decomposition in multiple synchronous reference frames,” *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1280–1289, July 2007.

[36] R. Teodorescu, F. Blaabjerg, U. Borup, and M. Liserre, “A new control structure for grid-connected lcl pv inverters with zero steady-state error and selective harmonic compensation,” in *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC ’04.*, vol. 1, Feb 2004, pp. 580–586 Vol.1.

[37] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid Synchronization in Single Phase Power Converters*. Wiley-IEEE Press, 2007.

[38] D. Stojic, N. Georgijevic, M. Rivera, and S. Milic, “Novel orthogonal signal generator for single phase pll applications,” *IET Power Electronics*, vol. 11, no. 3, pp. 427–433, 2018.

[39] Y. Han, M. Luo, X. Zhao, J. M. Guerrero, and L. Xu, “Comparative performance evaluation of orthogonal-signal-generators-based single-phase pll algorithms-a survey,” *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3932–3944, May 2016.

[40] Z. Ali, N. Christofides, L. Hadjidemetriou, E. Kyriakides, Y. Yang, and F. Blaabjerg, “Three-phase phase-locked loop synchronization algorithms for grid-connected renewable energy systems: A review,” *Renewable and Sustainable Energy Reviews*, vol. 90, pp. 434–452, 2018.

[41] J. Alipoor, Y. Miura, and T. Ise, “Power system stabilization using virtual synchronous generator with alternating moment of inertia,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 2, pp. 451–458, June 2015.

[42] H. Gu, Z. Yang, D. Wang, and W. Wu, “Research on control method of double-mode inverter with grid-connection and stand-alone,” in *2006 CES/IEEE 5th International Power Electronics and Motion Control Conference*, vol. 1, Aug 2006, pp. 1–5.

[43] Z. Yao, L. Xiao, and Y. Yan, “Seamless transfer of single-phase grid-interactive inverters between grid-connected and stand-alone modes,” *IEEE Transactions on Power Electronics*, vol. 25, no. 6, pp. 1597–1603, June 2010.

[44] M. Aten, G. Towers, C. Whitley, P. Wheeler, J. Clare, and K. Bradley, “Reliability comparison of matrix and other converter topologies,” *IEEE Transactions on Aerospace and Electronic Systems*, vol. 42, no. 3, pp. 867–875, July 2006.

[45] J. Qingzhong and W. Xingdou, “Research on high-speed communication technology between dsp and fpga,” in *2016 7th IEEE Control and System Graduate Research Colloquium (ICSGRC)*, Aug 2016, pp. 62–66.

[46] M. Hamouda, H. F. Blanchette, K. Al-Haddad, and F. Fnaiech, “An efficient dsp-fpga-based real-time implementation method of svm algorithms for an indirect matrix converter,” *IEEE Transactions on Industrial Electronics*, vol. 58, no. 11, pp. 5024–5031, Nov 2011.

[47] E. J. Bueno, A. Hernandez, F. J. Rodriguez, C. Giron, R. Mateos, and S. Cobreces, “A dsp- and fpga-based industrial control with high-speed communication interfaces for grid converters applied to distributed power generation systems,” *IEEE Transactions on Industrial Electronics*, vol. 56, no. 3, pp. 654–669, March 2009.

[48] Z. Chen, K. Wang, Z. Li, and T. Zheng, “A review on control strategies of ac/dc micro grid,” in *2017 IEEE International Conference on Environment and Electrical Engineering and 2017 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I CPS Europe)*, June 2017, pp. 1–6.

[49] A. Kazerooni, “LV Engine communications and data management requirements,” WSP, 2018.

[50] M. Liserre, G. Buticchi, M. Andresen, G. D. Carne, L. F. Costa, and Z. Zou, “The smart transformer: Impact on the electric grid and technology challenges,” *IEEE Industrial Electronics Magazine*, vol. 10, no. 2, pp. 46–58, June 2016.

[51] G. A. Klutke, P. C. Kiessler, and M. A. Wortman, “A critical look at the bathtub curve,” *IEEE Transactions on Reliability*, vol. 52, no. 1, pp. 125–129, March 2003.

[52] U. S. of America: Department of Defense, *Military Handbook: Reliability Prediction of Electronic Equipment: MIL-HDBK-217F: 2 December 1991*. Department of defense, 1991.

[53] Z.-Z. Elektrotechnik-und, “Handbook for robustness validation of automotive electrical/electronic modules,” 2013.

[54] N. R. Council *et al.*, *Reliability growth: enhancing defense system reliability*. National Academies Press, 2015.

[55] W. Weibull, “A statistical distribution function of wide applicability,” *Journal of Applied Mechanics*, vol. 18, no. 3, pp. 293–297, 1951.

[56] J. Falck, C. Felgemacher, A. Rojko, M. Liserre, and P. Zacharias, “Reliability of power electronic systems: An industry perspective,” *IEEE Industrial Electronics Magazine*, vol. 12, no. 2, pp. 24–35, June 2018.

[57] K. Ma, H. Wang, and F. Blaabjerg, “New approaches to reliability assessment: Using physics-of-failure for prediction and design in power electronics systems,” *IEEE Power Electronics Magazine*, vol. 3, no. 4, pp. 28–41, Dec 2016.

[58] C. Zhao, M. Weiss, A. Mester, S. Lewdeni-Schmid, D. Dujic, J. K. Steinke, and T. Chaudhuri, “Power electronic transformer (pet) converter: Design of a 1.2mw demonstrator for traction applications,” in *International Symposium on Power Electronics Power Electronics, Electrical Drives, Automation and Motion*, June 2012, pp. 855–860.

[59] M. Andresen, M. Schloh, G. Buticchi, and M. Liserre, “Computational light junction temperature estimator for active thermal control,” in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2016, pp. 1–7.

[60] M. Ciappa, “Selected failure mechanisms of modern power modules,” *Microelectronics Reliability*, vol. 42, no. 4, pp. 653 – 667, 2002. [Online]. Available: http://www.sciencedirect.com/-science/article/pii/S0026271402000422

[61] J. . Fabian, S. Hartmann, and A. Hamidi, “Analysis of insulation failure modes in high power igbt modules,” in *Fourtieth IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, 2005.*, vol. 2, Oct 2005, pp. 799–805 Vol. 2.

[62] M. Andresen, V. Raveendran, G. Buticchi, and M. Liserre, “Lifetime-based power routing in parallel converters for smart transformer application,” *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1675–1684, Feb 2018.

[63] Michel Olagnon and Zakoua Guede, “Rainflow fatigue analysis for loads with multimodel power spectral densities,” in *Marine Structures*, No. 2, Vol. 21, pp. 160–176, 2008.

[64] R. Alwitt and R. Hills, “The chemistry of failure of aluminum electrolytic capacitors,” *IEEE Transactions on Parts, Materials and Packaging*, vol. 1, no. 2, pp. 28–34, September 1965.

[65] Nippon Chemi-con, “Aluminum capacitors catalogue - technical note on judicious use of aluminum electrolytic capacitors,” *Tokyo, Japan*, 2013. [Online]. Available: http://www.chemi-con.com/2013AluminumElectrolyticCatalog.pdf

[66] Cornell Dubilier, “Aluminum electrolytic capacitor application guide,” *Liberty, SC, USA*. [Online]. Available: http://www.cde.com/catalogs/ AEappGUIDE.pdf

[67] A. Ritter, “Capacitor reliability issues and needs,” *presented at the Sandia Nat. Lab. Utility-Scale Grid-Tied PV Inverter Reliability Technical Workshop, Albuquerque, NM, USA*, Jan 2011.

[68] Q. Sun, Y. Tang, J. Feng, and T. Jin, “Reliability assessment of metallized film capacitors using reduced degradation test sample,” *Quality and Reliability Engineering International*, vol. 29, no. 2, pp. 259–265, Mar 2013.

[69] Nippon Chemi-con, “Power electronics film capacitors.” [Online]. Available: http://-www.kemet.com/kemet/web/homepage/kechome.nsf/weben/-AADFCC3E8AD80F8B85257713006A103F/*file*/ *F*9000*FilmPower.pdf*

[70] B. Rawal and N. Chan, “Conduction and failure mechanisms in barium titanate based ceramics under highly accelerated conditions,” in *Proceedings of the 34th Electronic Components Conference, New Orleans*, 1984, pp. 184–188.

[71] D. D. Liu and M. J. Sampson, “Some aspects of the failure mechanisms in batio3-based multilayer ceramic capacitors,” 2012.

[72] M. J. Cozzolino, “Electrical shorting in multilayer ceramic capacitors,” in *in Proc. CARTS Int.*, 2004, pp. 57–68.

[73] H. Wang, D. A. Nielsen, and F. Blaabjerg, “Degradation testing and failure analysis of dc film capacitors under high humidity conditions,” *Microelectronics Reliability*, vol. 55, no. 9, pp. 2007 – 2011, 2015, proceedings of the 26th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis. [Online]. Available: http://www.sciencedirect.com/-science/article/pii/S0026271415001419

[74] S. Bala, J. Pan, D. Das, O. Apeldoorn, and S. Ebner, “Lowering failure rates and improving serviceability in offshore wind conversion-collection systems,” in *2012 IEEE Power Electronics and Machines in Wind Applications*, July 2012, pp. 1–7.

[75] S. Jian, M. Xiaoqian, C. Shuying, and G. Huijing, “Review of the cooling technology for high-power wind turbines,” in *5th International Conference on Advanced Design and Manufacturing Engineering (ICADME 2015)*, 2015, pp. 1798–1803.

[76] V. Narayanaswamy, “A review of thermal and humidity management needs and feasible solutions for next generation subsea electric systems,” *Underwater Technology*, vol. 32, no. 2, pp. 129–143, Jan 2014.

[77] Semikron, “Application not an 16-001 effect of humidity and condensation on power electronics systems,” Semikron, Tech. Rep., 2016.

[78] H. Wang, M. Liserre, and F. Blaabjerg, “Toward reliable power electronics: Challenges, design tools, and opportunities,” *IEEE Industrial Electronics Magazine*, vol. 7, no. 2, pp. 17–26, June 2013.

[79] U. Scheuermann, “Increasing component reliability by eliminating solder interfaces,” in *2009 13th European Conference on Power Electronics and Applications*, Sept 2009, pp. 1–14.

[80] B. Ji, V. Pickert, W. Cao, and B. Zahawi, “In situ diagnostics and prognostics of wire bonding faults in igbt modules for electric vehicle drives,” *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5568–5577, Dec 2013.

[81] D. Barlini, M. Ciappa, A. Castellazzi, M. Mermet-Guyennet, and W. Fichtner, “New technique for the measurement of the static and of the transient junction temperature in igbt devices under operating conditions,” *Microelectronics Reliability*, vol. 46, no. 9, pp. 1772 – 1777, 2006, proceedings of the 17th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis. Wuppertal, Germany 3rdâ€“6th October 2006. [Online]. Available: http://-www.sciencedirect.com/science/article/pii/S0026271406002034

[82] H. Wang and F. Blaabjerg, “Reliability of capacitors for dc-link applications in power electronic converters—an overview,” *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3569–3578, Sept 2014.

[83] M. Andresen, “Active thermal control of power electronic modules in smart transformer applications,” Ph.D. dissertation, Kiel University, 2017.

[84] M. Andresen, L. F. Costa, G. Buticchi, and M. Liserre, “Smart transformer reliability and efficiency through modularity,” in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, May 2016, pp. 3241–3248.

[85] M. A. Brubaker, D. E. Hage, T. A. Hosking, H. C. Kirbie, and E. D. Sawyer, “Increasing the life of electrolytic capacitor banks using integrated high performance film capacitors,” in *presented at the Europe Power Conversion Intelligent Motion (PCIM), Nuremberg, Germany*, 2013.

[86] H. Wang, H. S. Chung, and W. Liu, “Use of a series voltage compensator for reduction of the dc-link capacitance in a capacitor-supported system,” *IEEE Transactions on Power Electronics*, vol. 29, no. 3, pp. 1163–1175, March 2014.

[87] R. Wang, F. Wang, D. Boroyevich, R. Burgos, R. Lai, P. Ning, and K. Rajashekara, “A high power density single-phase pwm rectifier with active ripple energy storage,” *IEEE Transactions on Power Electronics*, vol. 26, no. 5, pp. 1430–1443, May 2011.

[88] M. Chen, K. K. Afridi, and D. J. Perreault, “Stacked switched capacitor energy buffer architecture,” *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 5183–5195, Nov 2013.

[89] C. A. Walford, *Wind turbine reliability: understanding and minimizing wind turbine operation and maintenance costs*. United States. Department of Energy, 2006.

[90] “Regulatory investment test for distribution : Non-network options report,” 2018. [Online]. Available: https://www.ergon.com.au/__data/assets/pdf_file/0005/564377/Charleville-Non-Network-Options-Report.p

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